SBAS273 – DECEMBER 2002

Low-Power, 24-Bit ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **20-BIT EFFECTIVE RESOLUTION**
- **CURRENT CONSUMPTION: 90μA**
- **ANALOG SUPPLY: 2.5V to 5.25V**
- **DIGITAL SUPPLY: 1.8V to 3.6V**
- **±5V DIFFERENTIAL INPUT RANGE**
- **0.0002% INL (TYP), 0.0008% INL (MAX)**
- **SIMPLE 2-WIRE SERIAL INTERFACE**
- **SIMULTANEOUS 50Hz AND 60Hz REJECTION**
- **SINGLE CONVERSIONS WITH SLEEP MODE**
- **SINGLE-CYCLE SETTLING**
- **SELF-CALIBRATION**
- **WELL-SUITED FOR MULTICHANNEL SYSTEMS**
- **EASILY CONNECTS TO THE MSP430**

APPLICATIONS

- **HAND-HELD INSTRUMENTATION**
- **PORTABLE MEDICAL EQUIPMENT**
- **INDUSTRIAL PROCESS CONTROL**
- **WEIGH SCALES**

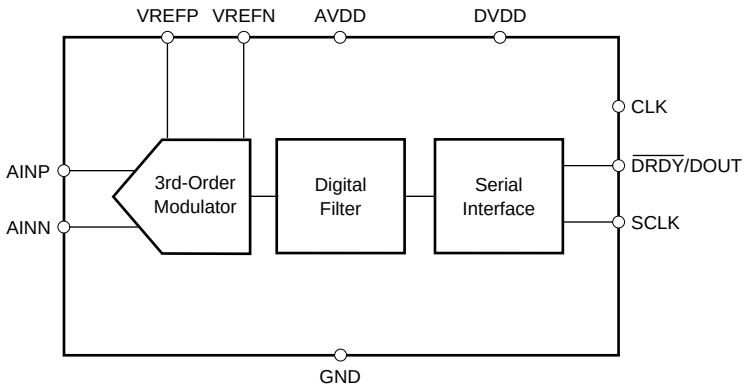
DESCRIPTION

The ADS1244 is a 24-bit, delta-sigma Analog-to-Digital (A/D) converter. It offers excellent performance and very low power in an MSOP-10 package and is well suited for demanding high-resolution measurements, especially in portable and other space- and power-constrained systems.

A 3rd-order delta-sigma modulator and digital filter form the basis of the A/D converter. The analog modulator has a ±5V differential input range. The digital filter rejects both 50Hz and 60Hz signals, completely settles in one cycle, and outputs data at 15 samples per second.

A simple, 2-wire serial interface provides all the necessary control. Data retrieval, self-calibration, and Sleep Mode are handled with a few simple waveforms. When only single conversions are needed, the ADS1244 can be shut down (Sleep Mode) while idle between measurements to dramatically reduce the overall power dissipation. Multiple ADS1244s can be connected together to create a synchronously sampling multichannel measurement system. The ADS1244 is designed to easily connect to microcontrollers, such as the MSP430.

The ADS1244 supports 2.5V to 5.25V analog supplies and 1.8V to 3.6V digital supplies. Power is typically less than 270μW in normal operation and less than 1μW during Sleep Mode.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS[1]

AVDD to GND	–0.3V to +6V
DVDD to GND	–0.3V to +3.6V
Input Current	100mA, Momentary
Input Current	10mA, Continuous
Analog Input Voltage to GND	–0.5V to AVDD + 0.5V
Digital Input Voltage to GND	–0.3V to DVDD + 0.3V
Digital Output Voltage to GND	–0.3V to DVDD + 0.3V
Maximum Junction Temperature	+150°C
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–60°C to +150°C
Lead Temperature (soldering, 10s)	+300°C

NOTE: (1) Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

DEMO BOARD ORDERING INFORMATION

PRODUCT	DESCRIPTION
ADS1244-EVM	ADS1244 Evaluation Module

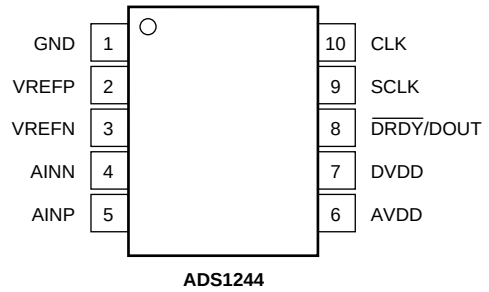
PACKAGE/ORDERING INFORMATION

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR[1]	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS1244	MSOP-10	DGS	–40°C to +85°C	BHG	ADS1244IDGST	Tape and Reel, 250
"	"	"	"	"	ADS1244IDGSR	Tape and Reel, 2500

NOTE: (1) For the most current specifications and package information, refer to our web site at www.ti.com.

PIN CONFIGURATION

Top View **MSOP**



ADS1244

PIN DESCRIPTIONS

PIN NUMBER	NAME	DESCRIPTION
1	GND	Analog and Digital Ground
2	VREFP	Positive Reference Input
3	VREFN	Negative Reference Input
4	AINN	Negative Analog Input
5	AINP	Positive Analog Input
6	AVDD	Analog Power Supply, 2.5V to 5.25V
7	DVDD	Digital Power Supply, 1.8V to 3.6V
8	$\overline{\text{DRDY}}$/DOUT	Dual-Purpose Output: Data Ready: Indicates valid data by going LOW. Data Output: Outputs data, MSB first, on the first rising edge of SCLK.
9	SCLK	Serial Clock Input: Clocks out data on the rising edge. Used to initiate calibration and Sleep Mode, see text for more details.
10	CLK	System Clock Input: Typically 2.4576MHz

ELECTRICAL CHARACTERISTICS

All specifications –40°C to +85°C, AVDD = 5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = 2.5V, unless otherwise specified.

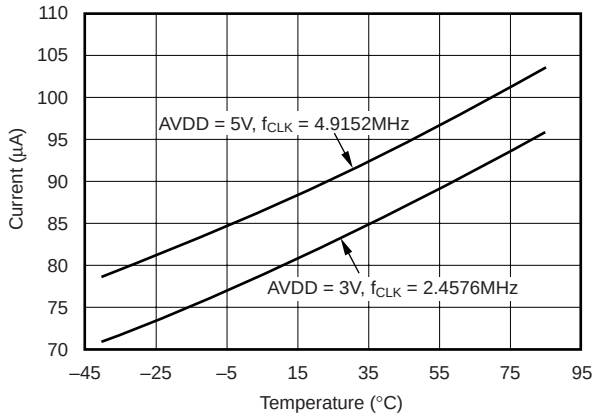
PARAMETER	CONDITIONS	ADS1244 MIN	ADS1244 TYP	ADS1244 MAX	UNITS
ANALOG INPUT					
Full-Scale Input Voltage Range	AINP – AINN		$\pm 2V_{REF}$		V
Absolute Input Range	AINP, AINN with Respect to GND	GND – 0.1		AVDD + 0.1	V
Differential Input Impedance	f_{CLK} = 2.4576MHz		5		MΩ
SYSTEM PERFORMANCE					
Resolution	No Missing Codes	24			Bits
Data Rate	f_{CLK} = 2.4576MHz		15		sps(1)
Integral Nonlinearity (INL)	Differential Input Signal, End Point Fit		±0.0002	±0.0008	% FSR(2)
Offset Error			1	10	ppm of FSR
Offset Error Drift(3)			0.01		ppm of FSR/°C
Gain Error			0.005	0.02	%
Gain Error Drift(3)			0.5		ppm/°C
Common-Mode Rejection	at DC	90	130		dB
	f_{CM}(4) = 50 ± 1Hz, f_{CLK} = 2.4576MHz	100			dB
	f_{CM} = 60 ± 1Hz, f_{CLK} = 2.4576MHz	100			dB
Normal-Mode Rejection	f_{SIG}(5) = 50 ± 1Hz, f_{CLK} = 2.4576MHz	60			dB
	f_{SIG} = 60 ± 1Hz, f_{CLK} = 2.4576MHz	70			dB
Input Referred Noise			1		ppm of FSR, rms
Analog Power-Supply Rejection	at DC, ΔAVDD = 5%		105		dB
Digital Power-Supply Rejection	at DC, ΔDVDD = 5%		100		dB
VOLTAGE REFERENCE INPUT					
Reference Input Voltage (V_{REF})	V_{REF} ≡ VREFP – VREFN	0.5	2.5	AVDD(6)	V
Negative Reference Input (VREFN)		GND – 0.1		VREFP – 0.5	V
Positive Reference Input (VREFP)		VREFN + 0.5		AVDD + 0.1	V
Voltage Reference Impedance	f_{CLK} = 2.4576MHz		1		MΩ
DIGITAL INPUT/OUTPUT					
Logic Levels					
V_{IH} (CLK, SCLK)		2.1		5.25	V
V_{IL} (CLK, SCLK)		GND		0.9	V
V_{OH} ($\overline{DRDY}$/DOUT)	I_{OH} = 1mA	2.6			V
V_{OL} ($\overline{DRDY}$/DOUT)	I_{OL} = 1mA			0.4	V
Input Leakage (CLK, SCLK)	0 < (CLK, SCLK) < DVDD			±10	µA
CLK Frequency (f_{CLK})				6	MHz
CLK Duty Cycle		30		70	%
POWER SUPPLY					
AVDD		2.5		5.25	V
DVDD		1.8		3.6	V
AVDD Current	Sleep Mode		0.1	1	µA
	AVDD = 3V		85		µA
	AVDD = 5V		90	150	µA
DVDD Current	Sleep Mode, CLK Stopped		0.1		µA
	Sleep Mode, 2.4576MHz CLK Running		1.3	5	µA
	DVDD = 3V		4.5	10	µA
Total Power Dissipation	AVDD = DVDD = 3V		270		µW

NOTES: (1) sps = Samples Per Second. (2) FSR = Full-Scale Range = $4V_{REF}$. (3) Recalibration can reduce these errors to the level of the noise. (4) f_{CM} is the frequency of the common-mode input. (5) f_{SIG} is the frequency of the input signal. (6) It will not be possible to reach the digital output full-scale code when V_{REF} > AVDD/2.

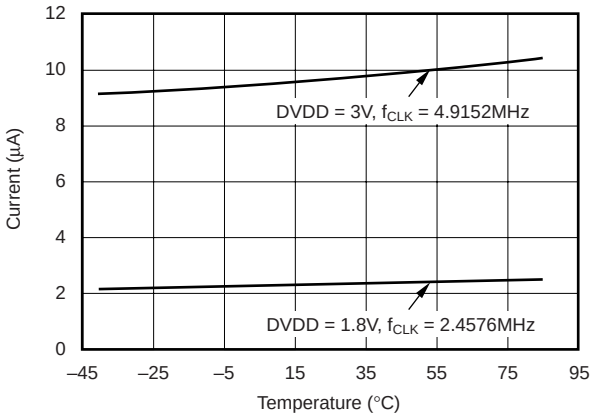
TYPICAL CHARACTERISTICS

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +2.5V, unless otherwise specified.

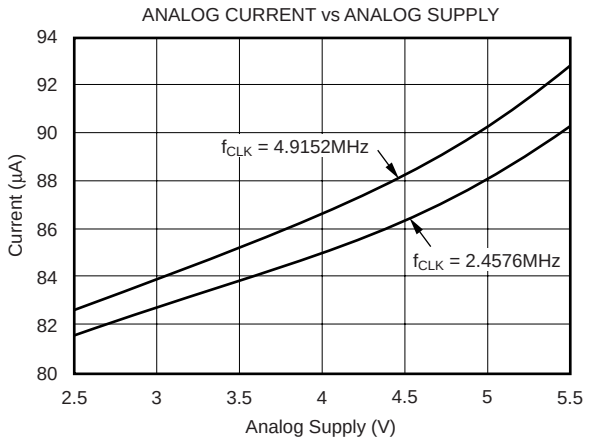
ANALOG CURRENT vs TEMPERATURE



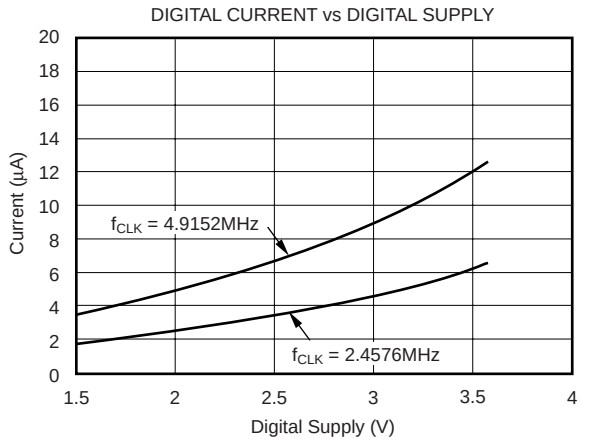
DIGITAL CURRENT vs TEMPERATURE



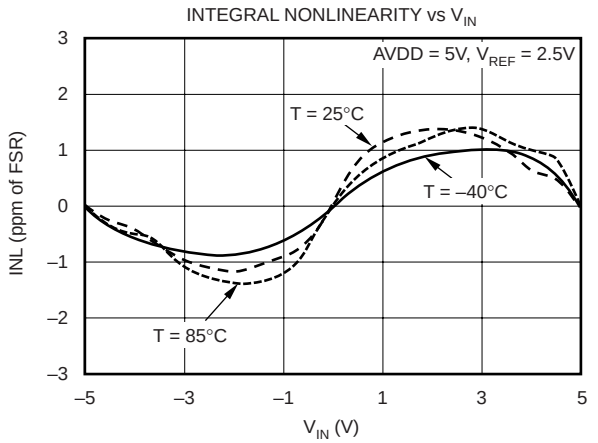
ANALOG CURRENT vs ANALOG SUPPLY



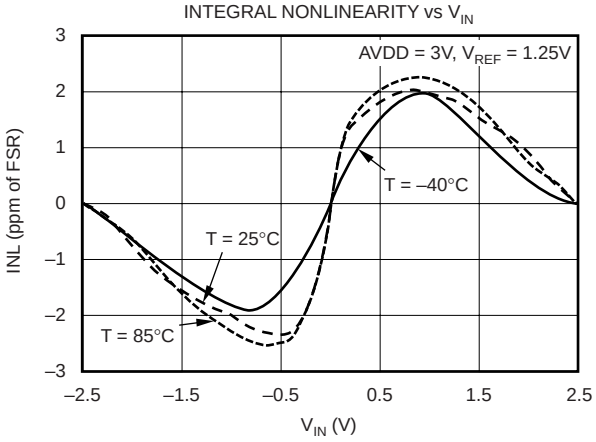
DIGITAL CURRENT vs DIGITAL SUPPLY



INTEGRAL NONLINEARITY vs V_{IN}



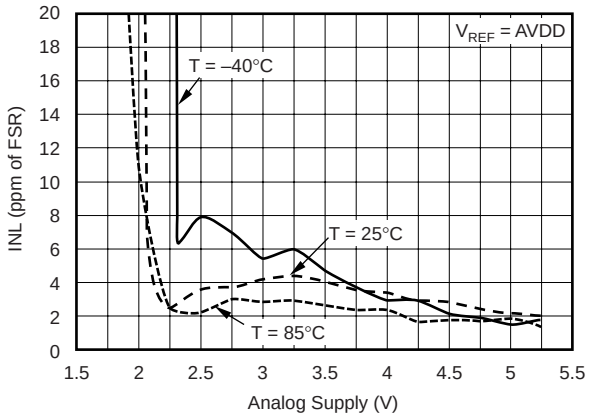
INTEGRAL NONLINEARITY vs V_{IN}



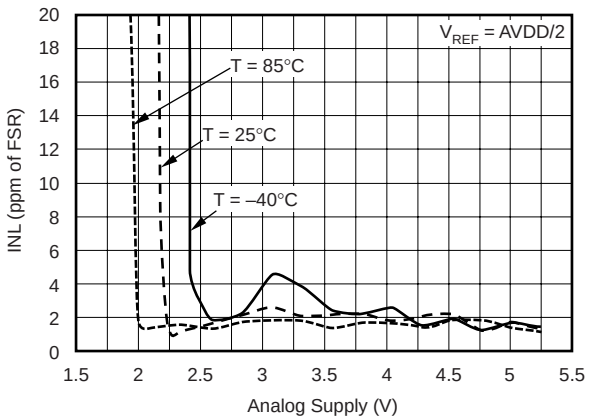
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +2.5V, unless otherwise specified.

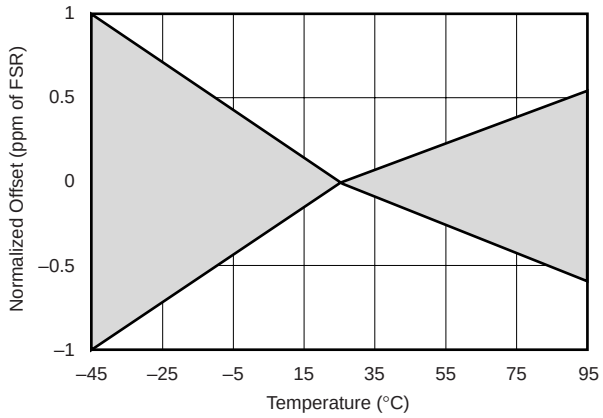
INTEGRAL NONLINEARITY vs ANALOG SUPPLY



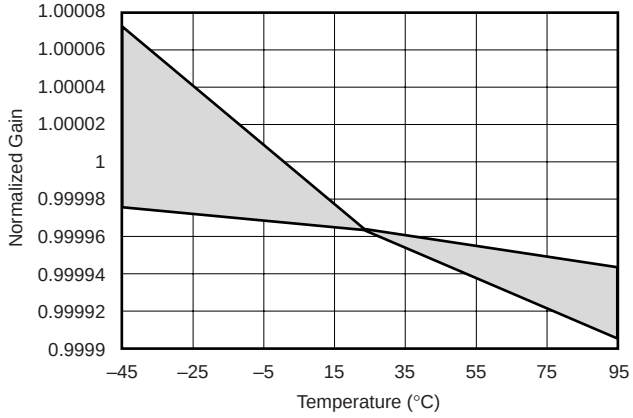
INTEGRAL NONLINEARITY vs ANALOG SUPPLY



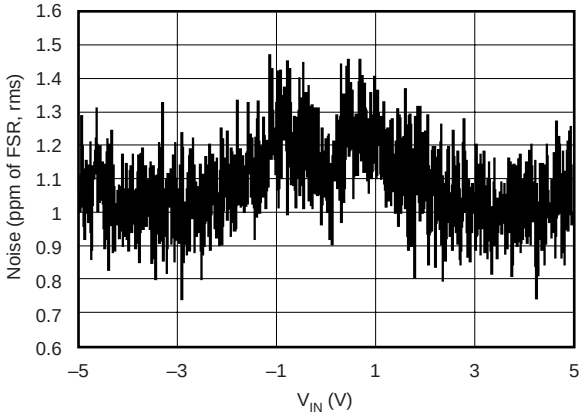
OFFSET vs TEMPERATURE



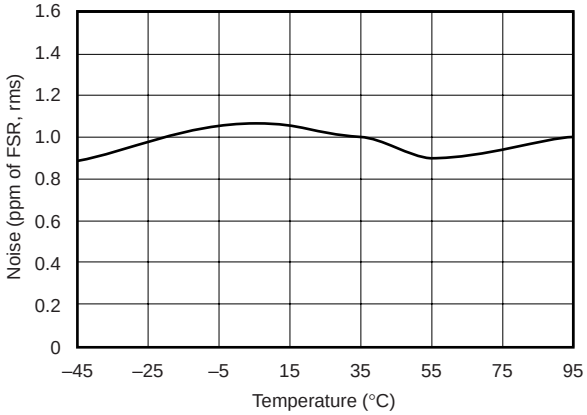
GAIN vs TEMPERATURE



NOISE vs INPUT SIGNAL



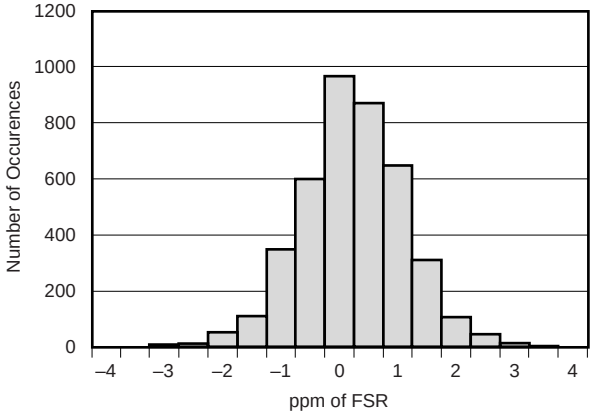
NOISE vs TEMPERATURE



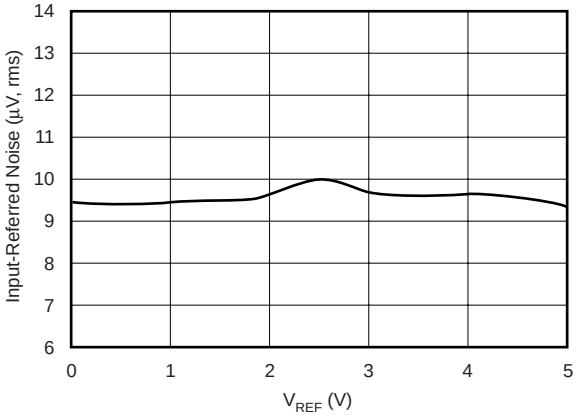
TYPICAL CHARACTERISTICS (Cont.)

At T_A = +25°C, AVDD = +5V, DVDD = +3V, f_{CLK} = 2.4576MHz, and V_{REF} = +2.5V, unless otherwise specified.

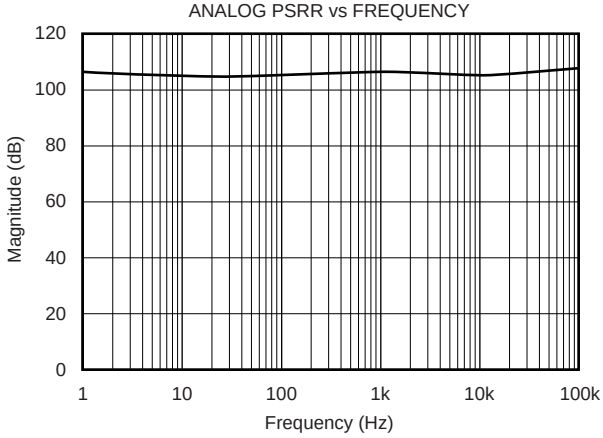
HISTOGRAM OF OUTPUT DATA



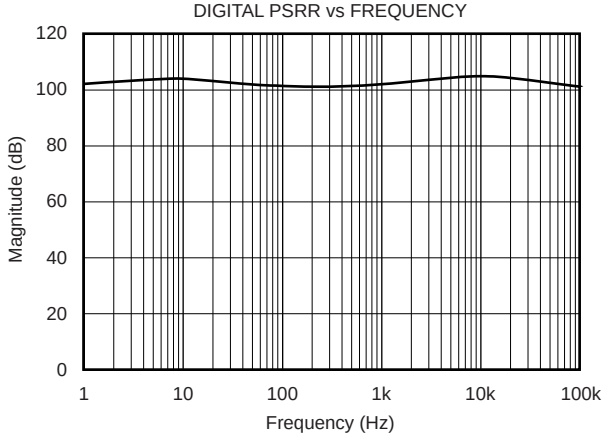
INPUT-REFERRED NOISE vs V_{REF}



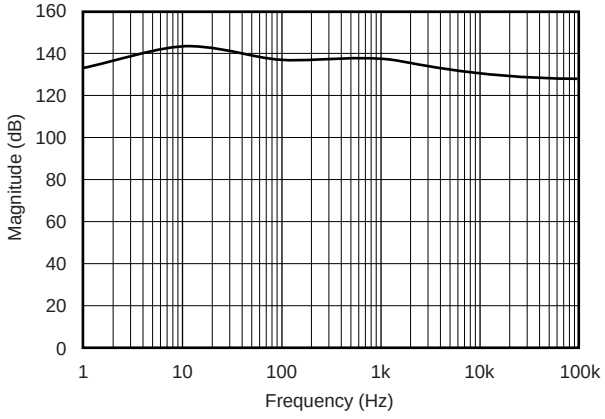
ANALOG PSRR vs FREQUENCY



DIGITAL PSRR vs FREQUENCY



CMRR vs FREQUENCY



OVERVIEW

The ADS1244 is an A/D converter comprised of a 3rd-order modulator followed by a digital filter. The modulator measures the differential input signal V_{IN} = (AINP – AINN) against the differential reference V_{REF} = (VREFP – VREFN). Figure 1 shows a conceptual diagram. The differential reference is scaled internally so that the full-scale input range is $\pm 2V_{REF}$. The digital filter receives the modulator's signal and provides a low-noise digital output. The filter also sets the frequency response of the converter and provides 50Hz and 60Hz rejection while settling in a single conversion cycle. A 2-wire serial interface indicates conversion completion and provides the user with the output data.

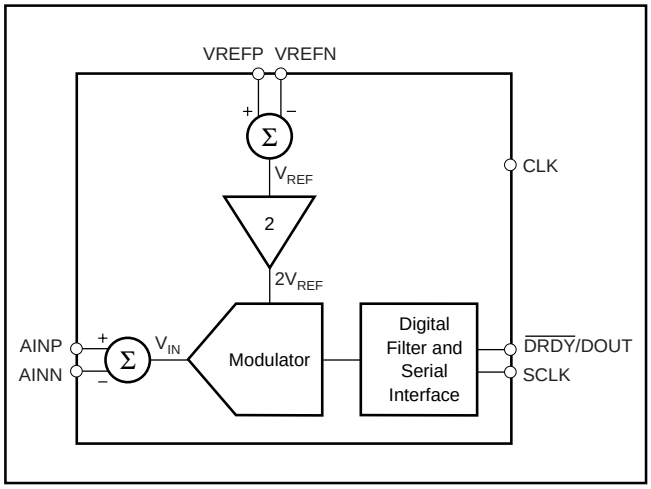


FIGURE 1. Conceptual Diagram of the ADS1244.

ANALOG INPUTS (AINP, AINN)

The input signal to be measured is applied to the input pins AINP and AINN. The ADS1244 accepts differential input signals, but can also measure unipolar signals. When measuring unipolar (or "single-ended" signals) with respect to ground, connect the negative input (AINN) to ground and connect the input signal to the positive input (AINP). Note that when the ADS1244 is used this way, only half of the converter's full-scale range is used since only positive digital output codes will be produced.

The ADS1244 measures the input signal using internal capacitors that are continuously charged and discharged. Figure 2 shows a simplified schematic of the ADS1244's input circuitry with Figure 3 showing the ON/OFF timings of the switches. S_1 switches close during the input sampling phase. With S_1 closed, C_{A1} charges to AINP, C_{A2} charges to AINN, and C_B charges to (AINP – AINN). For the discharge phase, S_1 opens first and then S_2 closes. C_{A1} and C_{A2} discharge to approximately AVDD/2 and C_B discharges to 0V. This 2-phase sample/discharge cycle repeats with a frequency of $f_{CLK}/128$ (19.2kHz for f_{CLK} = 2.4576MHz).

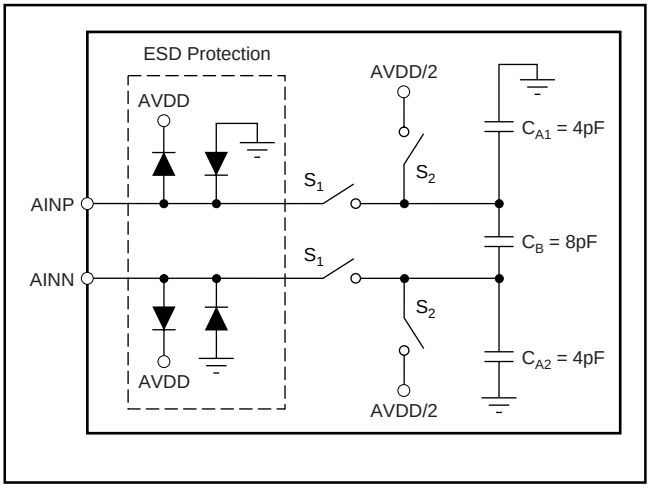


FIGURE 2. Simplified Input Structure.

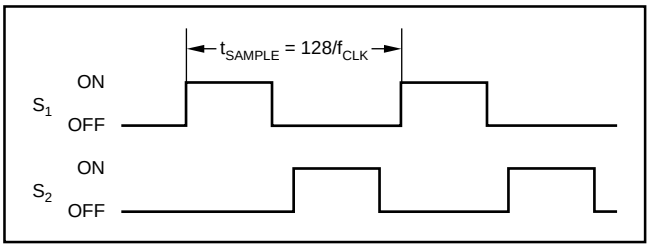


FIGURE 3. S_1 and S_2 Switch Timing for Figure 1.

The constant charging of the input capacitors presents a load on the inputs that can be represented by effective impedances. Figure 4 shows the input circuitry with the capacitors and switches of Figure 2 replaced by their effective impedances. These impedances scale inversely with f_{CLK} frequency. For example, if f_{CLK}'s frequency is reduced by a factor of 2, the impedances will double.

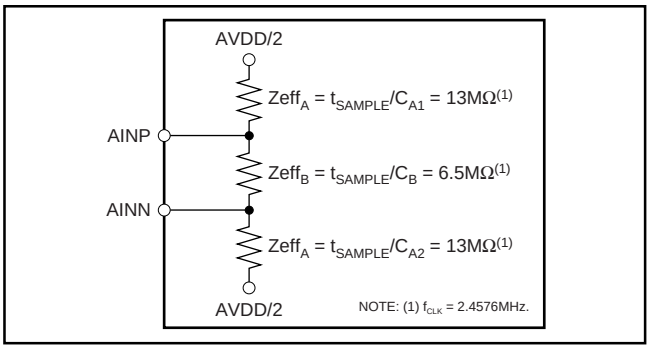


FIGURE 4. Effective Analog Input Impedances.

ESD diodes protect the inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below GND by more than 100mV, and likewise do not exceed AVDD by 100mV: GND – 100mV < (AINP, AINN) < AVDD + 100mV.

VOLTAGE REFERENCE INPUTS (VREFP, VREFN)

The voltage reference used by the modulator is generated from the voltage difference between VREFP and VREFN: V_{REF} = VREFP – VREFN. The reference inputs use a structure similar to that of the analog inputs. A simplified diagram of the circuitry on the reference inputs is shown in Figure 5. The switches and capacitors can be modeled with an effective impedance = $\left(\frac{t_{SAMPLE}}{2}\right) / 25pF = 1M\Omega$ for f_{CLK} = 2.4576MHz.

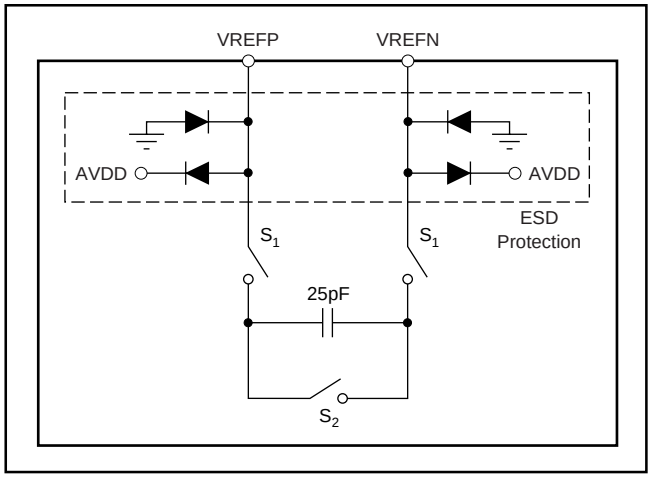


FIGURE 5. Simplified Reference Input Circuitry.

ESD diodes protect the reference inputs. To prevent these diodes from turning on, make sure the voltages on the reference pins do not go below GND by more than 100mV, and likewise do not exceed AVDD by 100mV: GND – 100mV < (VREFP, VREFN) < AVDD + 100mV.

V_{REF} is typically AVDD/2, but it can be raised as high as AVDD. When V_{REF} exceeds AVDD/2, it will not be possible to reach the full-scale digital output value corresponding to $\pm 2V_{REF}$ since this would require the analog inputs to exceed the power supplies. For example, if V_{REF} = AVDD = 5V, the positive full-scale signal is 10V. The maximum positive input signal that can be supplied before the ESD diodes begin to turn on is when AINP = 5.1V and AINN = –0.1V $\rightarrow$ V_{IN} = 5.2V. Therefore, it will not be possible to reach the positive (or negative) full-scale readings in this configuration. The digital output codes will be limited to approximately one half of the entire range.

For best performance, bypass the voltage reference inputs with a 0.1µF capacitor between VREFP and VREFN. Place the capacitor as close as possible to the pins.

CLOCK INPUT (CLK)

This digital input supplies the system clock to the ADS1244. The recommended CLK frequency is 2.4576MHz. This places the notches of the digital filter at 50Hz and 60Hz and sets the data rate at 15SPS. The CLK frequency can be increased to speed up the data rate, but the frequency notches will move in frequency proportionally. CLK must be left running during normal operation. It may be turned off during Sleep Mode to save power, but this is not required. The CLK input may be driven with 5V logic, regardless of the DVDD or AVDD voltage. Minimize the overshoot and undershoot on CLK for the best analog performance. A small resistor in series with CLK (10Ω to 100Ω) can often help. CLK can be generated from a number of sources including stand-alone crystal oscillators and microcontrollers. The MSP430, an ultra low power microcontroller, is especially well suited for this task. Using the MSP430's FLL clock generator available on the 4xx family, it's easy to produce a 2.4576MHz clock from a 32.768kHz crystal.

DATA READY/DATA OUTPUT ($\overline{DRDY}$/DOUT)

This digital output pin serves two purposes. It indicates when new data is ready by going LOW. Afterwards, on the first rising edge of SCLK, the $\overline{DRDY}$/DOUT pin changes function and begins outputting the conversion data, MSB first. Data is shifted out on each subsequent SCLK rising edge. After all 24 bits have been retrieved, the pin can be forced HIGH with an additional SCLK. It will then stay HIGH until new data is ready. This is useful when polling on the status of $\overline{DRDY}$/DOUT to determine when to begin data retrieval.

SERIAL CLOCK INPUT (SCLK)

This digital input shifts serial data out with each rising edge. As with CLK, this input may be driven with 5V logic regardless of the DVDD or AVDD voltage. There is hysteresis built into this input, but care should still be taken to ensure a clean signal. Glitches or slow rising signals can cause unwanted additional shifting. For this reason, it is best to make sure the rise-and-fall times of SCLK are less than 50ns.

FREQUENCY RESPONSE

The ADS1244's frequency response for f_{CLK} = 2.4576MHz is shown in Figure 6. The frequency response repeats at multiples of 19.2kHz. The overall response is that of a low-pass filter with a –3dB cutoff frequency of 13.7Hz. As can be seen, the ADS1244 does a good job attenuating out to 19kHz. For the best resolution, limit the input bandwidth to below this value to keep higher frequency noise from affecting performance. Often a simple RC filter on the ADS1244's analog inputs is all that is needed.

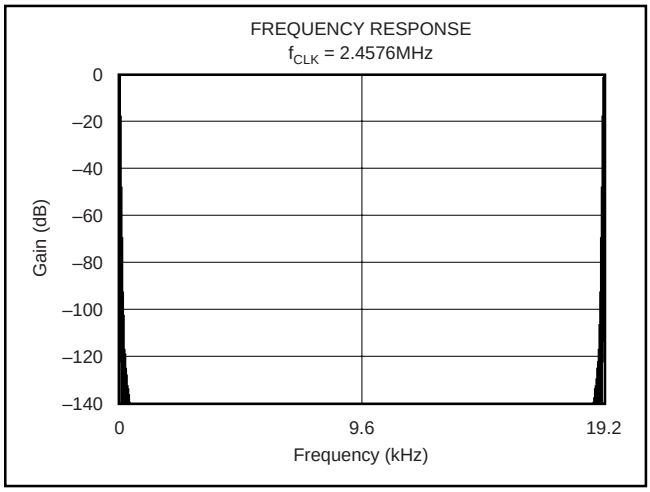


FIGURE 6. Frequency Response.

To help see the response at lower frequencies, Figure 7 illustrates the response out to 180Hz. Notice that both 50Hz and 60Hz signals are rejected. This feature is very useful for eliminating power line cycle interference during measurements. Figure 8 shows the ADS1244's response around these frequencies.

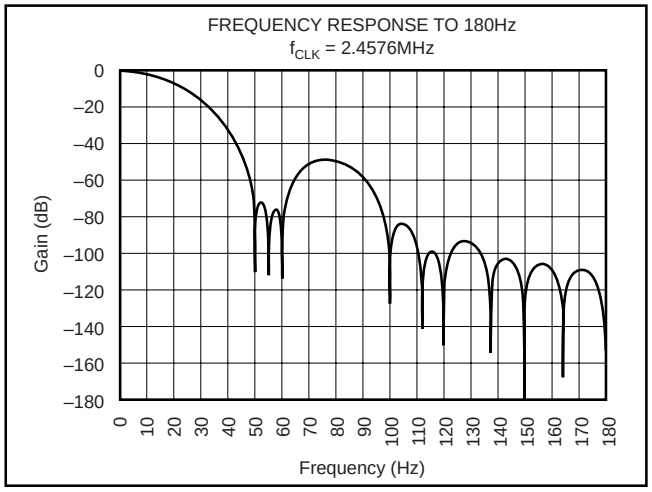


FIGURE 7. Frequency Response to 180Hz.

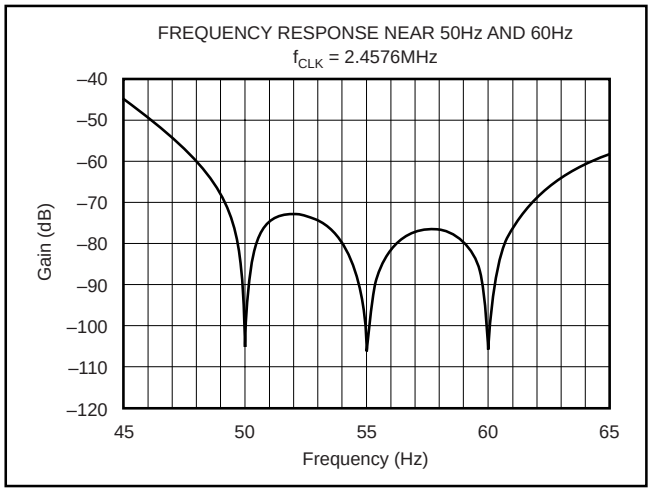


FIGURE 8. Frequency Response Near 50Hz and 60Hz.

The ADS1244's data rate and frequency response scale directly with CLK frequency. For example, if f_{CLK} increases from 2.4576MHz to 4.9152MHz, the data rate increases from 15sps to 30sps while the notches in the response at 50Hz and 60Hz move out to 100Hz and 120Hz.

SETTLING TIME

The ADS1244 has single-cycle settling. That is, the output data is fully settled after a single conversion—there is no need to wait for additional conversions before retrieving the data when there is a change on the analog inputs.

In order to realize single-cycle settling, synchronize changes on the analog inputs to the conversion beginning, which is indicated by the falling edge of $\overline{DRDY}$/DOUT. For example, when using a multiplexer in front of the ADS1244, change the multiplexer's inputs when $\overline{DRDY}$/DOUT goes LOW. Increasing the time between the conversion beginning and the change on the analog inputs (t_{DELAY}) will result in a settling error in the conversion data, as shown in Figure 9. The settling error versus delay time is shown in Figure 10. If the input change is delayed to the point where the settling error is too high, simply ignore the first data result and wait for the second conversion which will be fully-settled.

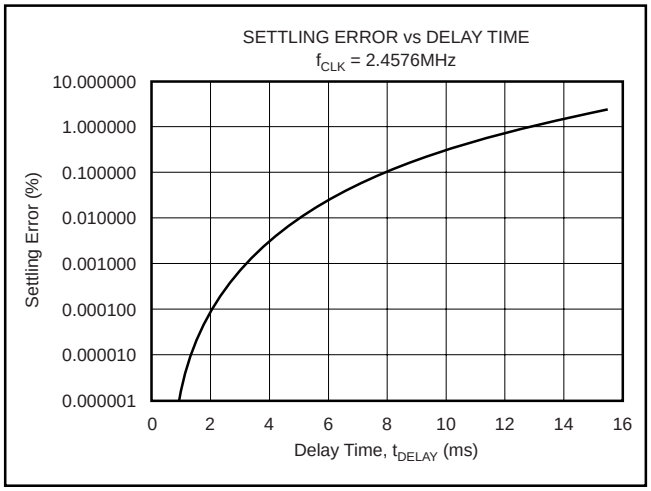


FIGURE 10. Settling Error vs Delay Time.

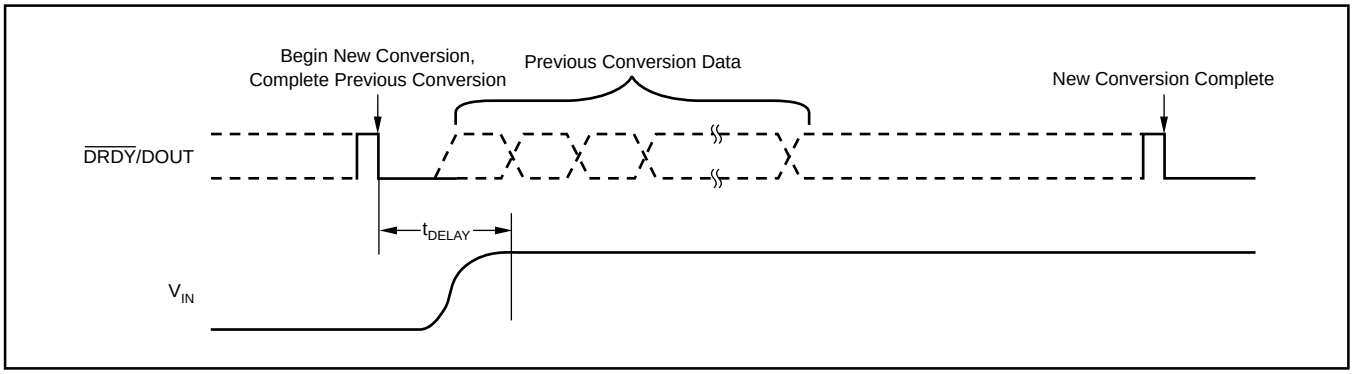


FIGURE 9. Analog Input Change Timing.

POWER-UP

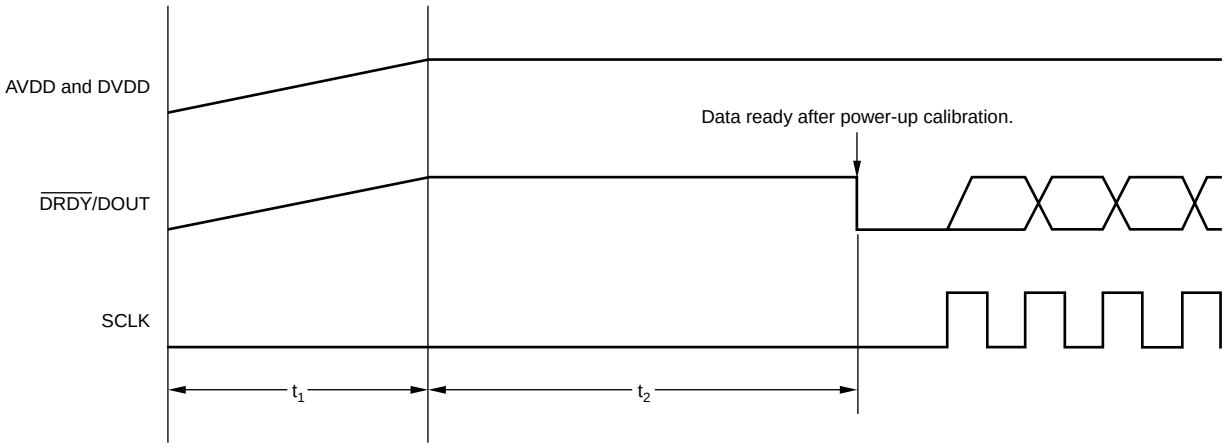
Self-calibration is performed at power-up to minimize offset and gain errors. In order for the self-calibration at power-up to work properly, make sure that both AVDD and DVDD increase monotonically and are settled by t_1, as shown in Figure 11. SCLK must be held LOW during this time. Once calibration is complete, $\overline{DRDY}$/DOUT will go LOW indicating data is ready for retrieval. The time required before the first data is ready (t_6) depends on how fast AVDD and DVDD ramp to their final value (t_1). For most ramp rates, $t_1 + t_2 \approx 350ms$ (f_{CLK} = 2.4576MHz). If the system environment is not stable during power-up (the temperature is varying or the supply voltages are moving around), it is recommended that a self-calibration be issued after everything is stable.

DATA FORMAT

The ADS1244 outputs 24 bits of data in Binary Two's Complement format. The Least Significant Bit (LSB) has a weight of $(2V_{REF})/(2^{23} - 1)$. A positive full-scale input produces an output code of $7FFFFF_H$ and the negative full-scale input produces an output code of 800000_H. The output clips at these codes for signals exceeding full-scale. Table I summarizes the ideal output codes for different input signals.

INPUT SIGNAL V_{IN} (AINP – AINN)	IDEAL OUTPUT CODE(1)
$\geq +2V_{REF}$	$7FFFFF_H$
$\frac{+2V_{REF}}{2^{23} - 1}$	000001_H
0	000000_H
$\frac{-2V_{REF}}{2^{23} - 1}$	$FFFFFF_H$
$\leq -2V_{REF}\left(\frac{2^{23}}{2^{23} - 1}\right)$	800000_H
NOTE: (1) Excludes effects of noise, INL, offset, and gain errors.	

TABLE I. Ideal Output Code versus Input Signal.



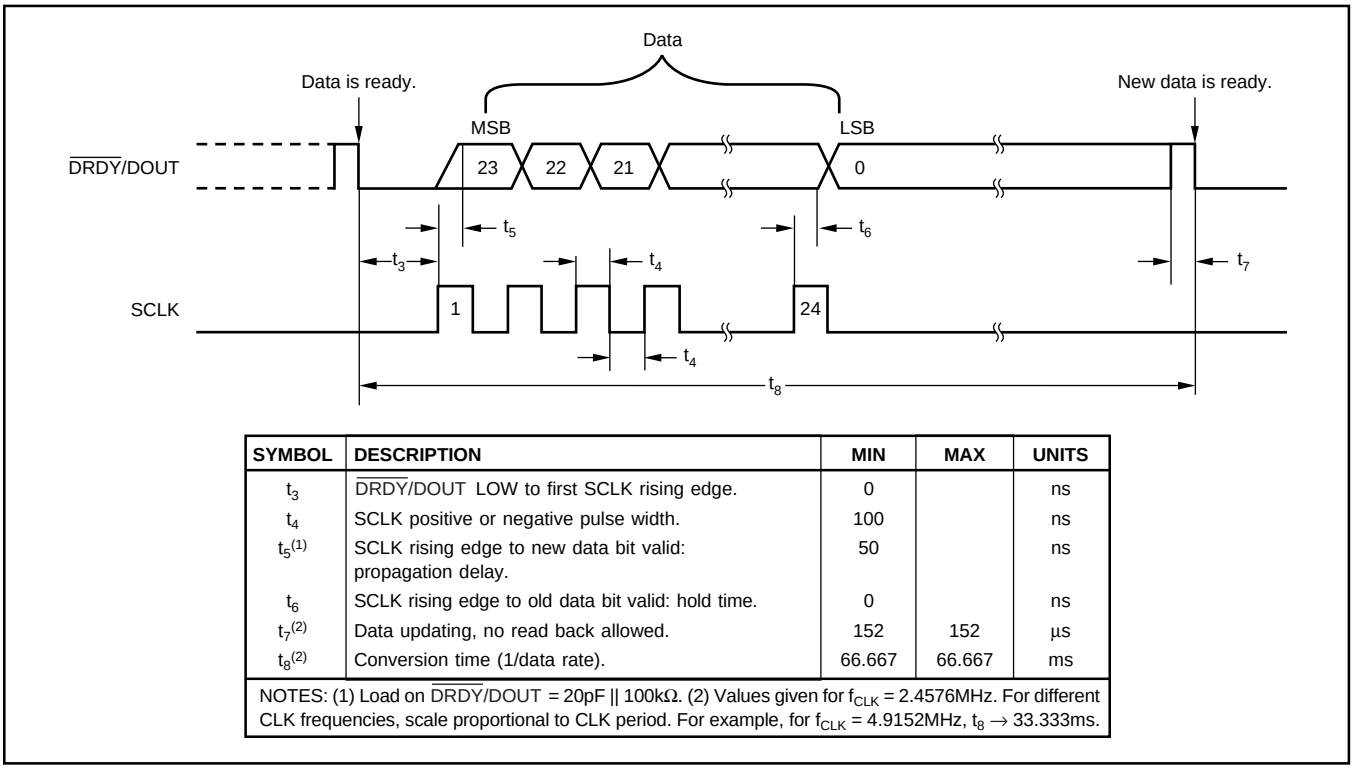
SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_1(1)	AVDD and DVDD settling time.		100	ms
t_2(1)	Wait time for calibration and first data conversion.	316		ms
NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.				

FIGURE 11. Power-Up Timing.

DATA RETRIEVAL

The ADS1244 continuously converts the analog input signal. To retrieve data, wait until $\overline{DRDY}$/DOUT goes LOW, as shown in Figure 12. After this occurs, begin shifting out the data by applying SCLKs. Data is shifted out Most Significant Bit (MSB) first. It is not required to shift out all the 24 bits of data, but the data must be retrieved before the new data is updated (see t_3) or else it will be overwritten. Avoid data retrieval during the update period. $\overline{DRDY}$/DOUT will remain at the state of the last bit shifted out until it is taken HIGH (see t_7), indicating that new data is being updated.

To avoid having $\overline{DRDY}$/DOUT remain in the state of the last bit, shift a 25th SCLK to force $\overline{DRDY}$/DOUT HIGH, see Figure 13. This technique is useful when a host controlling the ADS1244 is polling $\overline{DRDY}$/DOUT to determine when data is ready.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_3	$\overline{DRDY}$/DOUT LOW to first SCLK rising edge.	0		ns
t_4	SCLK positive or negative pulse width.	100		ns
t_5(1)	SCLK rising edge to new data bit valid: propagation delay.	50		ns
t_6	SCLK rising edge to old data bit valid: hold time.	0		ns
t_7(2)	Data updating, no read back allowed.	152	152	µs
t_8(2)	Conversion time (1/data rate).	66.667	66.667	ms

NOTES: (1) Load on $\overline{DRDY}$/DOUT = 20pF || 100kΩ. (2) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period. For example, for f_{CLK} = 4.9152MHz, $t_8 \rightarrow$ 33.333ms.

FIGURE 12. Data Retrieval Timing.

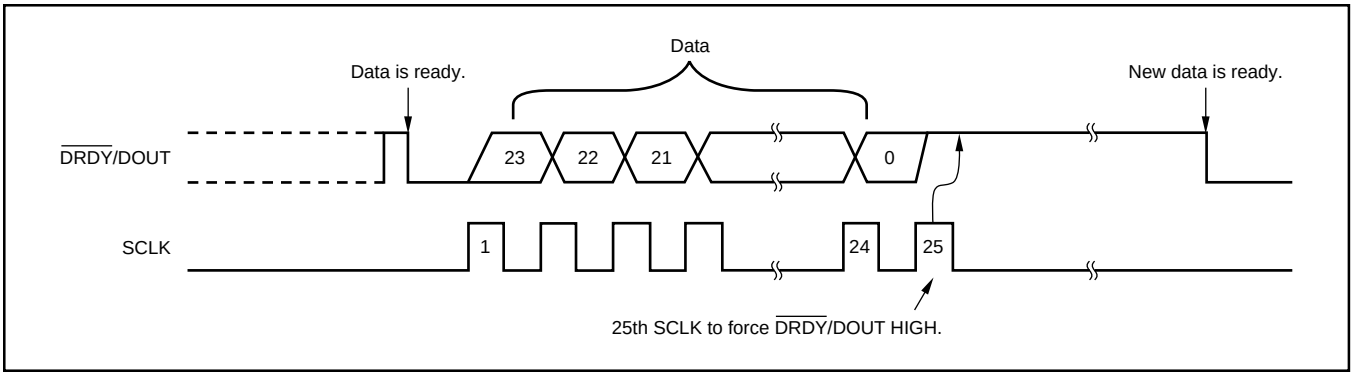
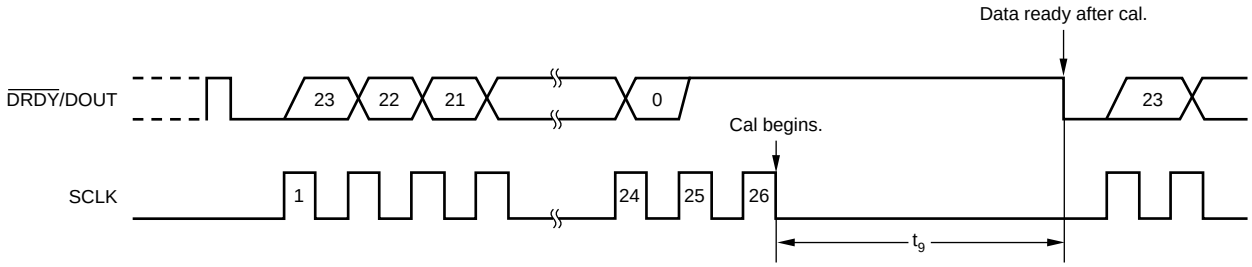


FIGURE 13. Data Retrieval with $\overline{DRDY}$/DOUT Forced HIGH Afterwards.

SELF-CALIBRATION

The user can initiate self-calibration at any time, though in many applications the ADS1244's drift performance is good enough that the self-calibration performing automatically at power-up is all that is needed. To initiate a self-calibration, apply at least two additional SCLKs after retrieving 24 bits of data. Figure 14 shows the timing pattern. The 25th SCLK will send $\overline{\text{DRDY}}$/DOUT HIGH. The falling edge of the 26th SCLK will begin the calibration cycle. Additional SCLK pulses may be sent after the 26th SCLK, but try to minimize activity on SCLK during calibration for best results.

When the calibration is complete, $\overline{\text{DRDY}}$/DOUT will go LOW indicating that new data is ready. There is no need to alter the analog input signal applied to the ADS1244 during calibration, the inputs pins are disconnected within the A/D converter and the appropriate signals applied internally automatically. The first conversion after a calibration is fully settled and valid for use. The time required for a calibration depends on two independent signals: the falling edge of SCLK and an internal clock derived from CLK. Variations in the internal calibration values will change the time required for calibration (t_9) within the range given by the MIN/MAX specs. t_{12} and t_{13} described in the next section are affected likewise.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_9(1)	First data ready after calibration.	209	210	ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

FIGURE 14. Self-Calibration Timing.

SLEEP MODE

Sleep Mode dramatically reduces power consumption (typically < 1µW with CLK stopped) by shutting down all of the active circuitry. To enter Sleep Mode, simply hold SCLK HIGH after $\overline{DRDY}$/DOUT goes LOW, as shown in Figure 15. Sleep Mode can be initiated at any time during read back; it is not necessary to retrieve all 24 bits of data beforehand. Once t_{11} has passed with SCLK held HIGH, Sleep Mode will activate. $\overline{DRDY}$/DOUT stays HIGH once Sleep Mode begins. SCLK must remain HIGH to stay in Sleep Mode. To exit Sleep Mode ("wakeup"), set SCLK LOW. The first data after exiting Sleep Mode is valid. It is not necessary to stop CLK during Sleep Mode, but doing so will further reduce the digital supply current.

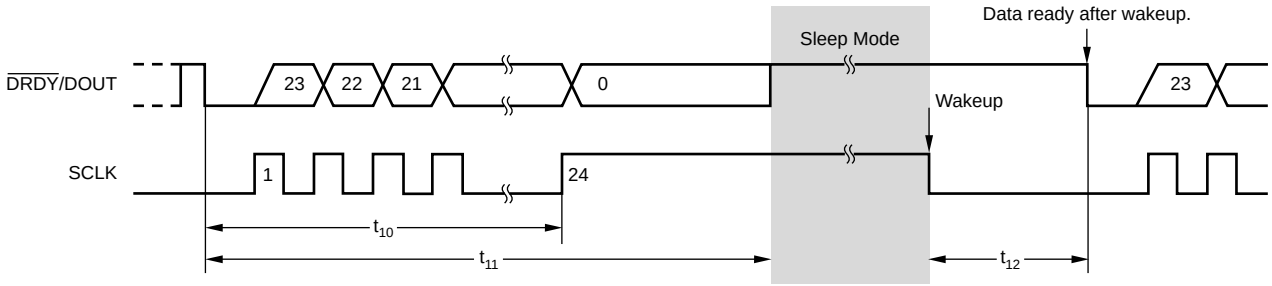
Sleep Mode With Self-Calibration

Self-calibration can be set to run immediately after exiting Sleep Mode. This is useful when the ADS1244 is put in Sleep Mode for long periods of time and self-calibration is desired afterwards to compensate for temperature or supply voltage changes.

To force a self-calibration with Sleep Mode, shift 25 bits out before taking SCLK HIGH to enter Sleep Mode. Self-calibration will then begin after wakeup. Figure 16 shows the appropriate timing. Note the extra time needed after wakeup for calibration before data is ready. The first data after Sleep Mode with self-calibration is fully-settled and can be used.

SINGLE CONVERSIONS

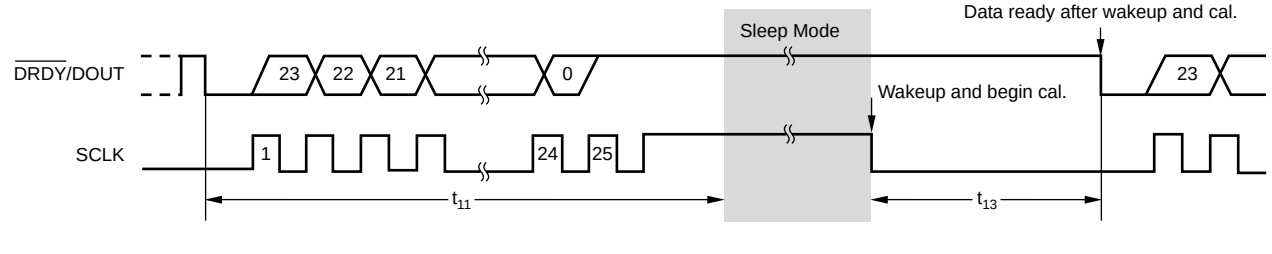
When only single conversions are needed, Sleep Mode can be used to start and stop the ADS1244. To make a single conversion, first enter the Sleep Mode holding SCLK HIGH. Now, when ready to start the conversion, take SCLK LOW. The ADS1244 will wake up and begin the conversion. Wait for $\overline{DRDY}$/DOUT to go LOW, and then retrieve the data. Afterwards, take SCLK HIGH to stop the ADS1244 from converting and re-enter Sleep Mode. Continue to hold SCLK HIGH until ready to start the next conversion. Operating in this fashion greatly reduces power consumption since the ADS1244 is shut down while idle between conversions. Self-calibrations can be performed prior to the start of the single conversions by using the waveform shown in Figure 16.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{10}(1)	SCLK HIGH after $\overline{DRDY}$/DOUT goes LOW to activate Sleep Mode.	0	63.7	ms
t_{11}(1)	Sleep Mode activation Time.	66.5	66.5	ms
t_{12}(1)	Data ready after wakeup.	71	72	ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

FIGURE 15. Sleep Mode Timing; Can be Used for Single Conversions.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{13}(1)	Data ready after wakeup and calibration.	210	211	ms

NOTE: (1) Values given for f_{CLK} = 2.4576MHz. For different CLK frequencies, scale proportional to CLK period.

FIGURE 16. Sleep Mode with Self-Calibration on Wakeup Timing; Can be Used for Single Conversions.

SINGLE-SUPPLY OPERATION

It is possible to operate the ADS1244 with a single supply. For a 3V supply, simply connect AVDD and DVDD together. Figure 17 shows an example of the ADS1244 running on a single 5V supply. An external resistor, R1, is used to drop 5V supply down to a desired voltage level of DVDD. For example, if the desired DVDD supply voltage is 3V and AVDD is 5V, the value of R1 should be:

$$R1 = (5V - 3V)/4.5\mu A \approx 440k\Omega$$

where 4.5µA is a typical digital current consumption when DVDD = 3V (refer to the typical characteristic "Digital Current vs Digital Supply"). A buffer on $\overline{DRDY}$/DOUT can provide level-shifting if required.

DVDD can be set to a desired voltage by choosing a proper value of R1, but keep in mind that DVDD must be set between 1.8V and 3.6V. Note that the maximum logic HIGH output of $\overline{DRDY}$/DOUT is equal to DVDD, but both CLK and SCLK inputs can be driven with 5V logic regardless of the DVDD or AVDD voltage. Use 0.1µF capacitors to bypass both AVDD and DVDD.

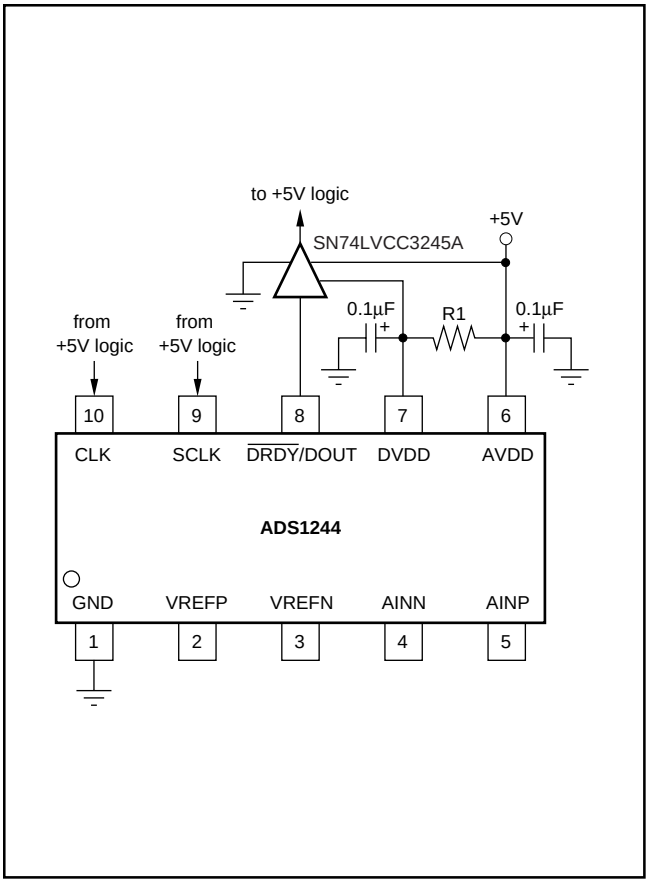
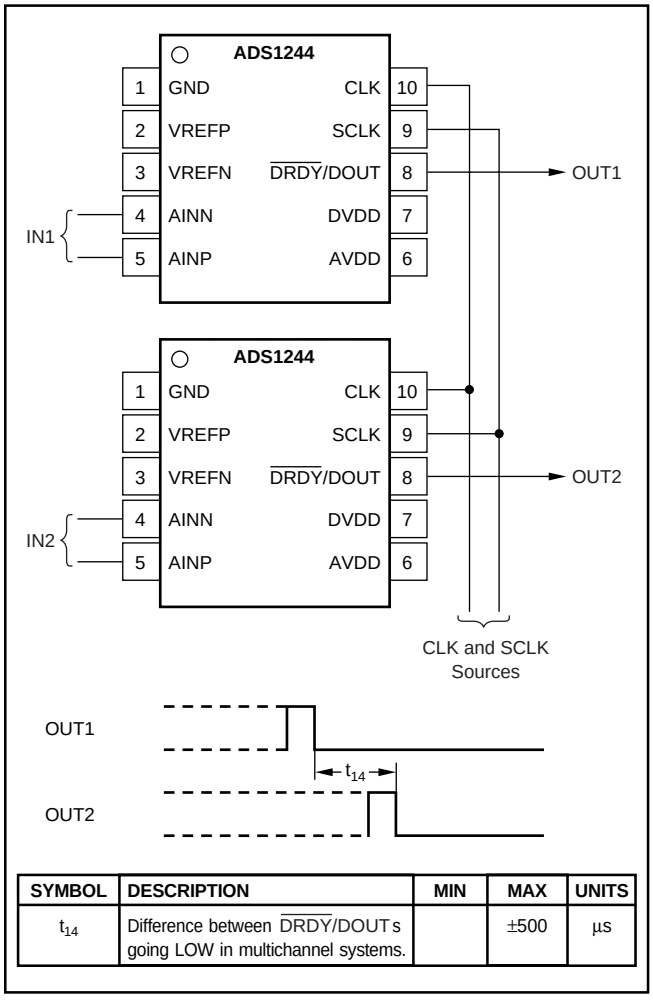


FIGURE 17. Example of the ADS1244 Running on a Single 5V Supply.

MULTICHANNEL SYSTEMS

Multiple ADS1244s can be operated in parallel to measure multiple input signals. Figure 18 shows an example of a 2-channel system. For simplicity, the supplies and reference circuitry were not included. The same CLK signal should be applied to all devices. To be able to synchronize the ADS1244s, connect the same SCLK signal to all devices as well. When ready to synchronize, place all the devices in Sleep Mode. Afterwards, "wakeup" and all the ADS1244s will be synchronized. That is, they will sample the input signals simultaneously.

The $\overline{DRDY}$/DOUT outputs will go LOW at approximately the same time after synchronization. The falling edges indicating that new data is ready will vary with respect to each other no more than timing specification t_{14}. This variation is due to posible differences in the ADS1244's internal calibration settings. To account for this when using multiple devices, either wait for t_{14} to pass after seeing one device's $\overline{DRDY}$/DOUT go LOW, or wait until all $\overline{DRDY}$/DOUTs have gone LOW before retrieving data.



SYMBOL	DESCRIPTION	MIN	MAX	UNITS
t_{14}	Difference between $\overline{DRDY}$/DOUTs going LOW in multichannel systems.		±500	µs

FIGURE 18. Example of Using Multiple ADS1244s in Parallel.

WEIGH SCALE SYSTEM

Figure 19 shows an example of a weigh scale system. OPA1, OPA2, R_G, and R_F form a differential gain stage to amplify the load cell output. The gain is equal to $(1 + 2\ R_F/R_G)$. Depending on the load cell, the typical gain setting is from 100 to 250. R_I and C_I form a single-pole low-pass filter to band-limit the differential gain stage noise and reduce mechanical vibration noise from the load cell. The cutoff frequency of the low-pass filter should be as low as possible to minimize the overall system noise. The reference voltage is typically generated by dividing down the supply voltage (R_{VR1}, R_{VR2}). Use a bypass capacitor located as close to VREFP as possible.

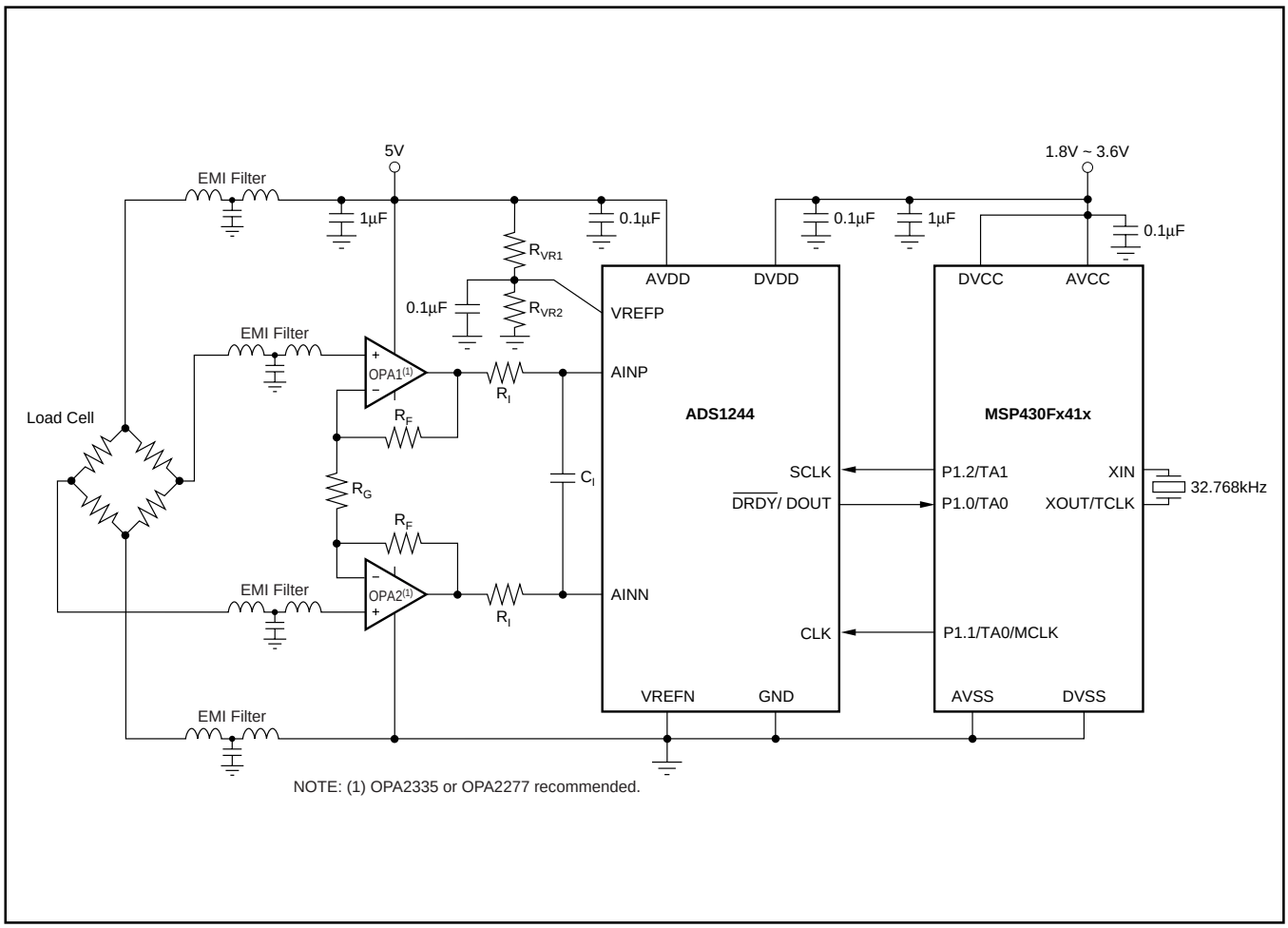


FIGURE 19. Weigh Scale System.

SUMMARY OF SERIAL INTERFACE WAVEFORMS

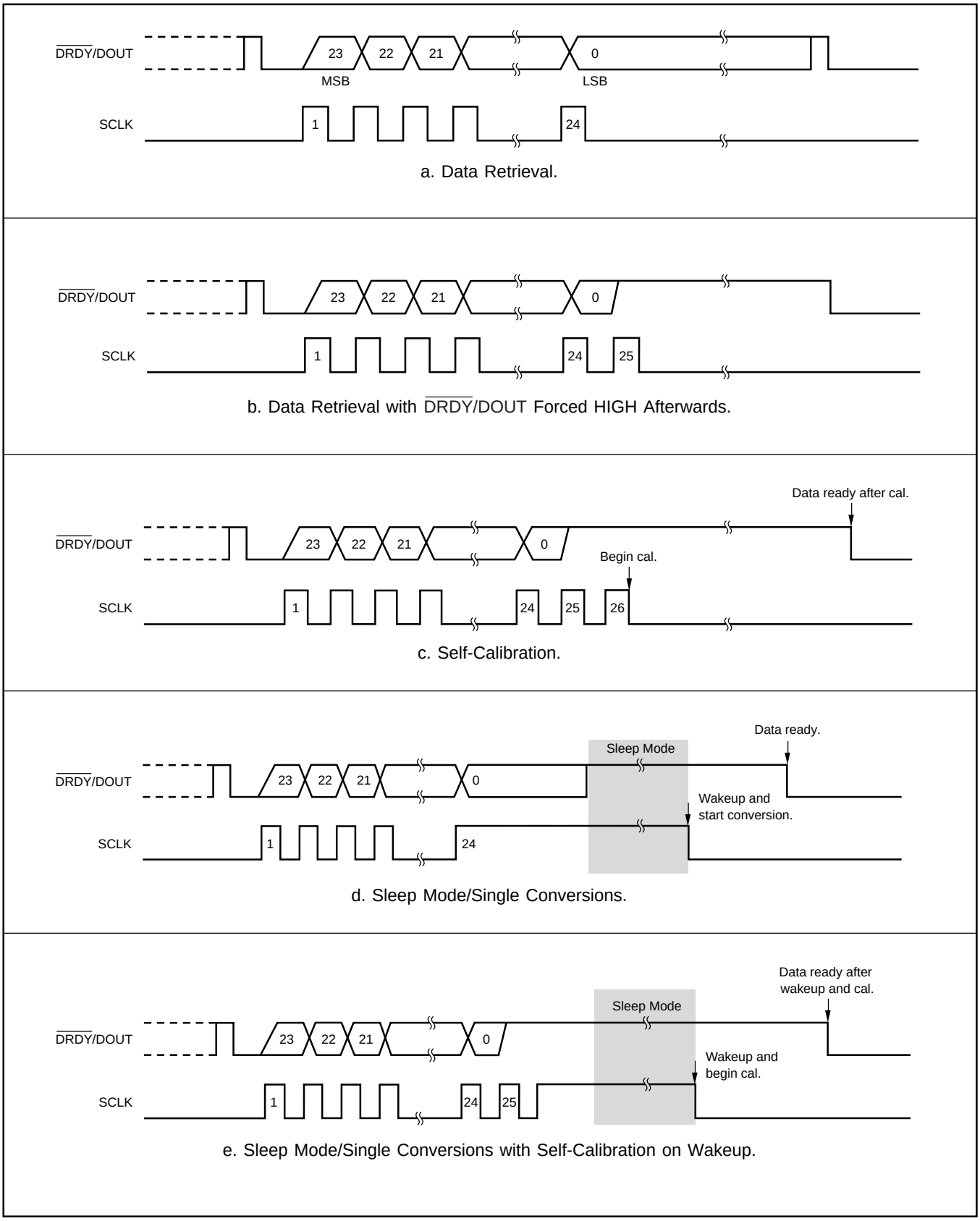
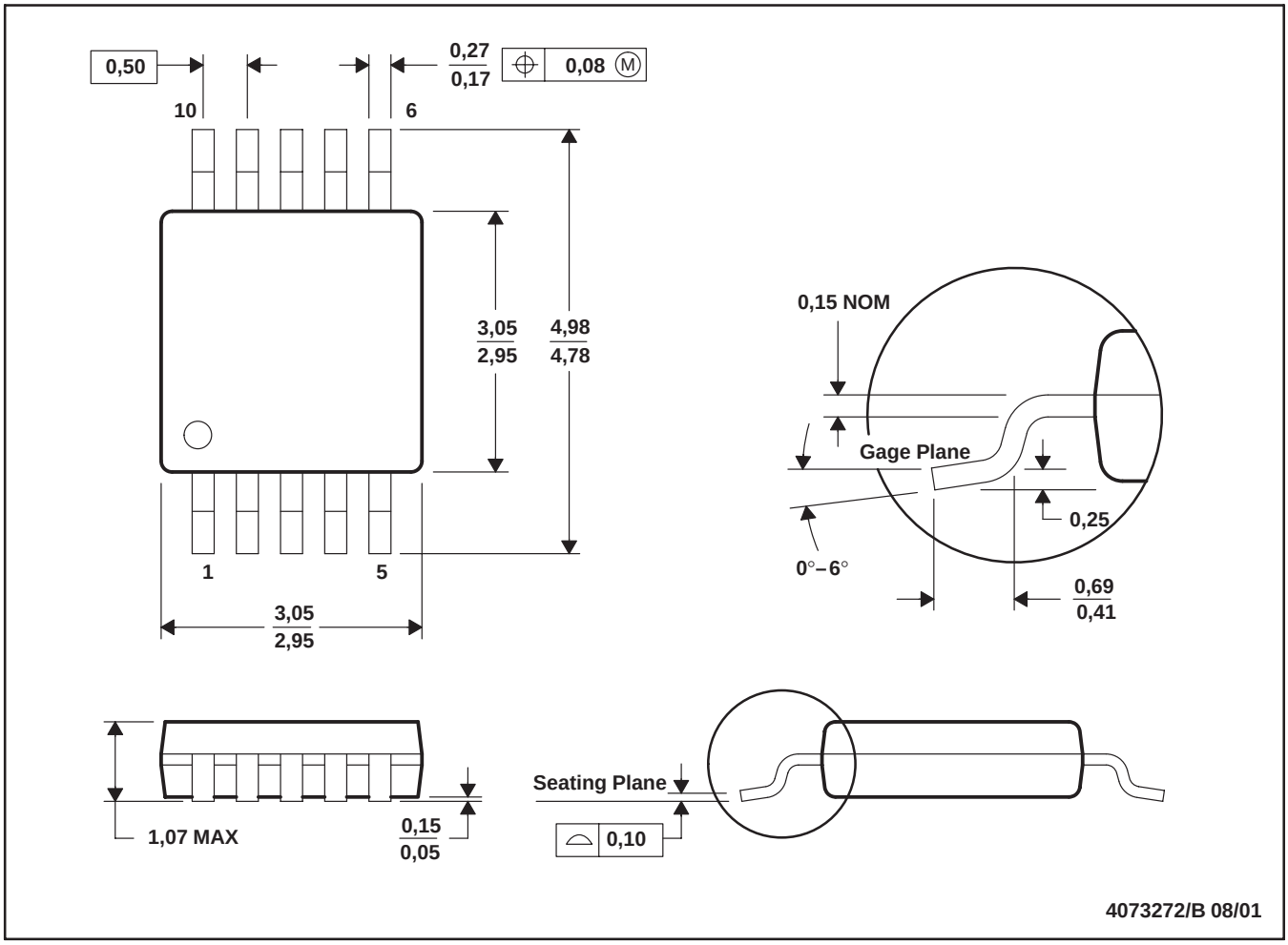


FIGURE 20. Summary of Serial Interface Waveforms.

DGS (S-PDSO-G10) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
A. Falls within JEDEC MO-187

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
ADS1244IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHG	Samples
ADS1244IDGSRG4	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHG	Samples
ADS1244IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHG	Samples
ADS1244IDGSTG4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	BHG	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

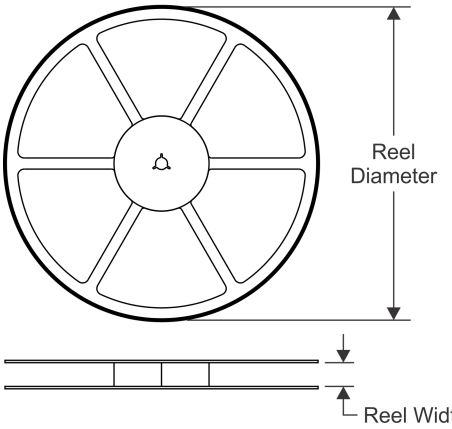
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

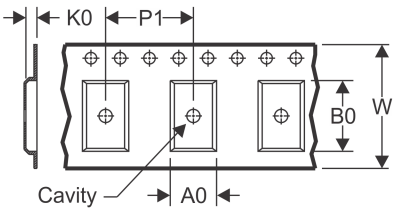
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

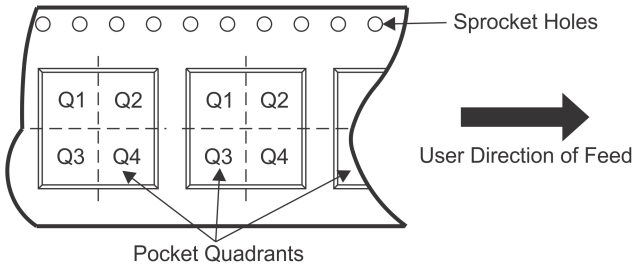


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

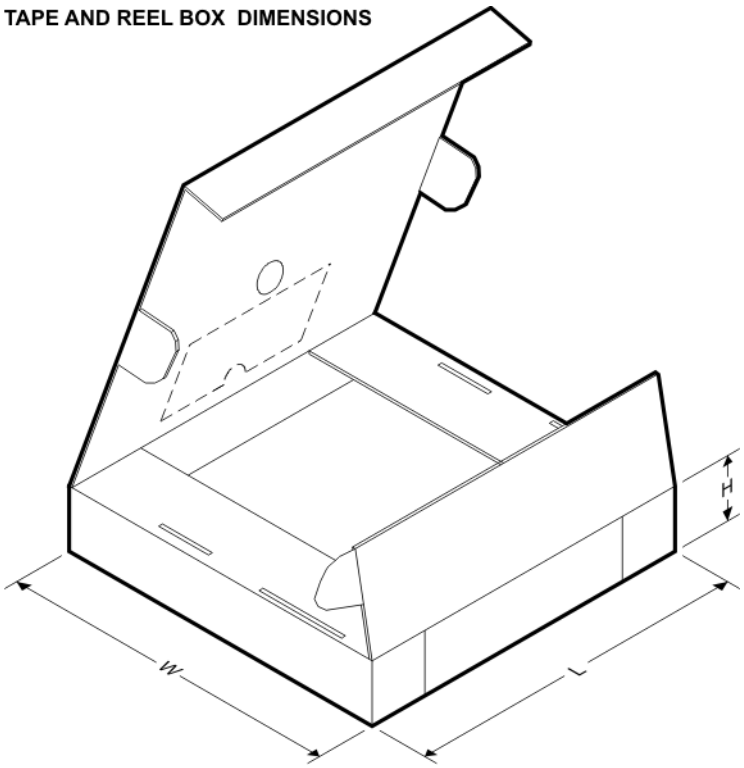
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1244IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS1244IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

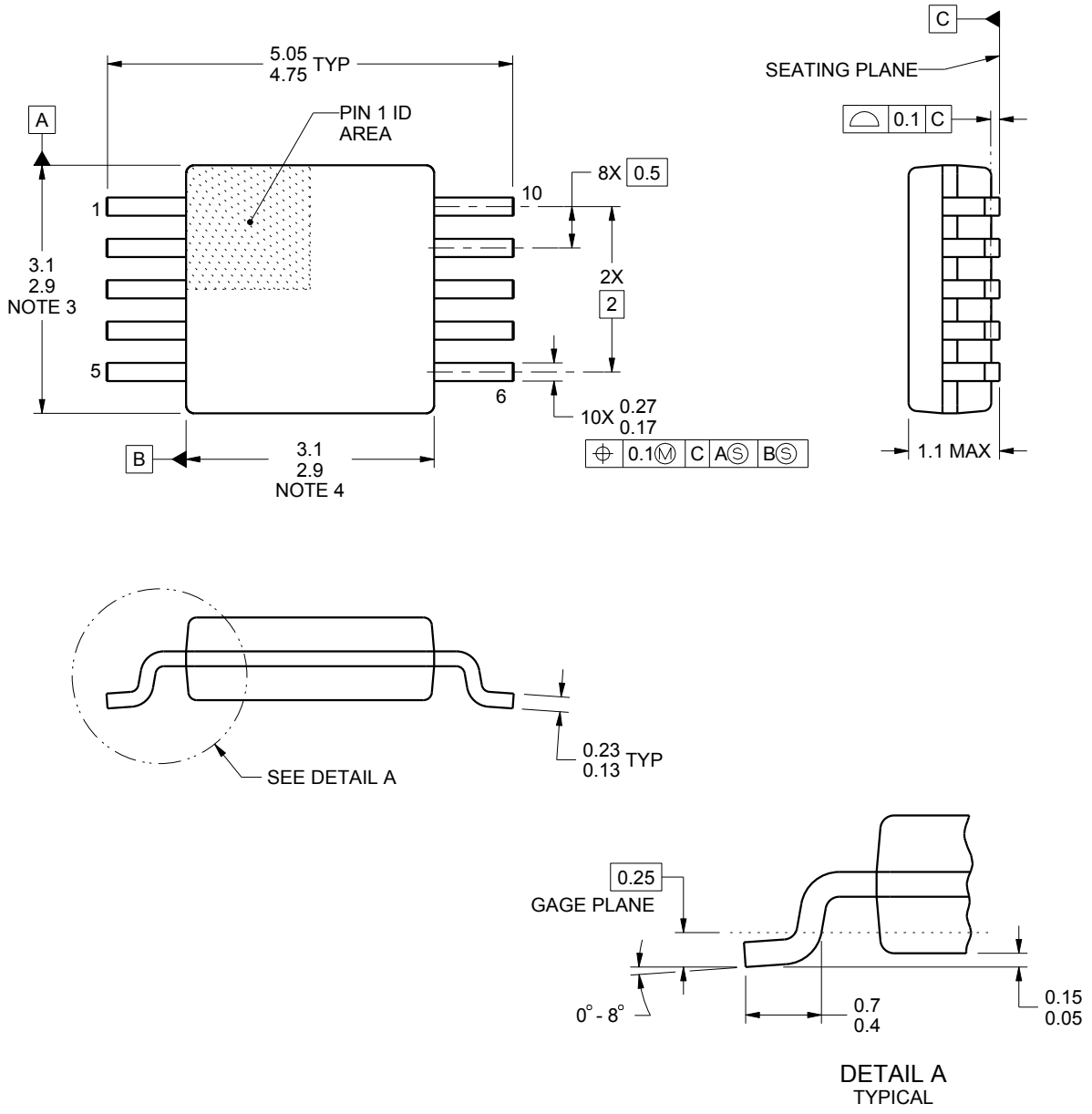
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1244IDGSR	VSSOP	DGS	10	2500	367.0	367.0	35.0
ADS1244IDGST	VSSOP	DGS	10	250	210.0	185.0	35.0

PACKAGE OUTLINE

DGS0010A

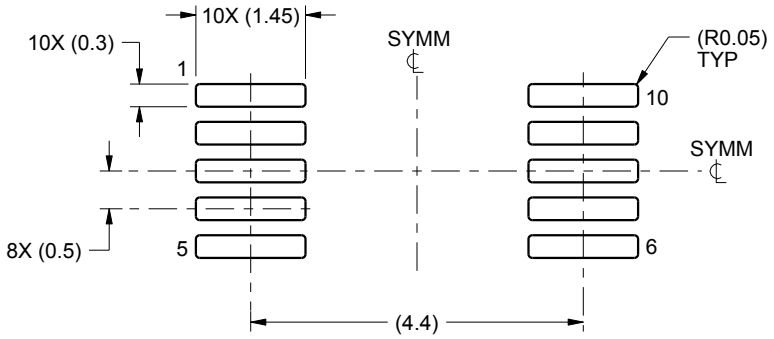
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

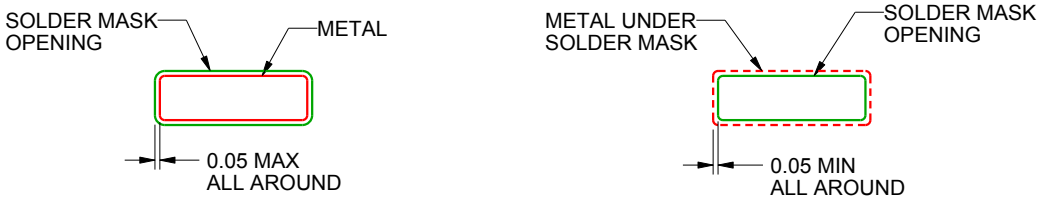


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

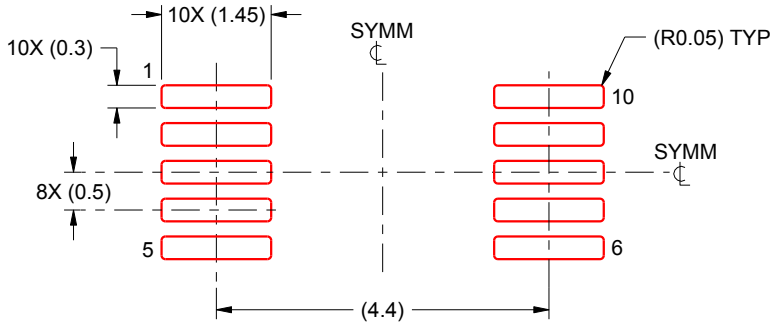


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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