16-Bit, 40kSPS, Low-Power Sampling ANALOG-TO-DIGITAL CONVERTER with Internal Reference and Parallel/Serial Interface

FEATURES

- 40kSPS Minimum Sampling Rate
- Very Low Power: 24mW Typ
- ±3.33V, ±5V, ±10V, 4V, and 10V Input Ranges
- 89dB SNR with 10kHz Input
- ±2LSB Max INL
- –1/+2LSB Max DNL, 16-Bit NMC
- ±10mV BPZ, ±2.5ppm/°C BPZ Drift
- 89dB Min SINAD, 102dB Min SFDR
- Uses Internal or External 2.5V Reference
- No External Calibration Resistors Required
- Single 5V Analog Supply:
  - 32.5mW Max Power Dissipation
  - 50μW Max Power-Down Mode
- SPI™-Compatible Serial Port up to 20MHz, with Master/Slave Feature
- Global CONV and 3-Stated Bus for Multi-Chip Simultaneous S/H Operation
- Pin-Compatible with 16-Bit ADS7813 and 12-Bit ADS7812 and ADS8512
- SO-16 Package

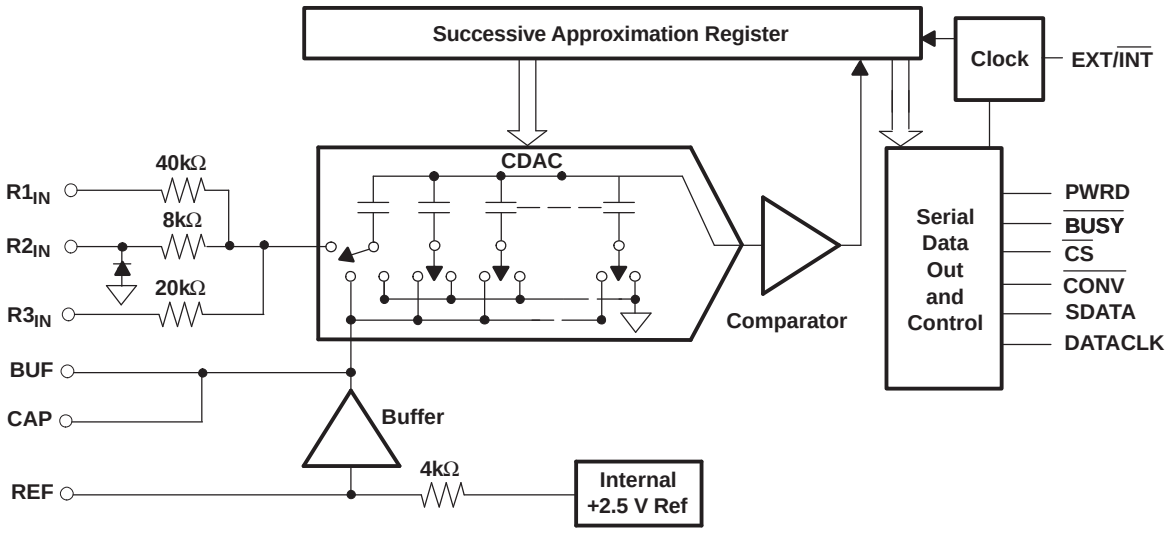
APPLICATIONS

- Industrial Process Control
- Test Equipment
- Robotics
- DSP Servo Control
- Medical Instrumentation
- Portable Data Acquisition Systems

DESCRIPTION

The ADS8513 is a complete low-power, single 5V supply, 16-bit sampling analog-to-digital (A/D) converter. It contains a complete 16-bit capacitor-based, successive approximation register (SAR) A/D converter with sample and hold, clock, reference, and serial data interface. The converter can be configured for a variety of input ranges including ±10V, ±5V, 0V to 10V, and 0.5V to 4.5V. A high-impedance, 0.3V to 2.8V input is also available with input impedance greater than 10MΩ. For most input ranges, the input voltage can swing to 25V or –25V without damage to the converter.

An SPI-compatible serial interface allows data to be synchronized to an internal or external clock. The ADS8513 is specified at 40kSPS sampling rate over the –40°C to +85°C industrial temperature range.



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MINIMUM INL (LSB)	NO MISSING CODES	MINIMUM SINAD (dB)	SPECIFIED TEMPERATURE RANGE	PACKAGE LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QTY
ADS8513IB	±2	16-Bit	89	–40°C to +85°C	SO-16	DW	ADS8513IBDW	Tube, 20
							ADS8513IBDWR	Tape and Reel, 1000
ADS8513I	±3	15-Bit	88	–40°C to +85°C	SO-16	DW	ADS8513IDW	Tube, 20
							ADS8513IDWR	Tape and Reel, 1000

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted).

PARAMETER		UNIT
Analog inputs	$R1_{IN}$	±25V
	$R2_{IN}$	±25V
	$R3_{IN}$	±25V
	REF	V_S + 0.3V to GND – 0.3V
Ground voltage differences	GND	±0.3V
	V_S	6V
Digital inputs		–0.3V to +V_S + 0.3V
Maximum junction temperature		+165°C
Storage temperature range		–65°C to +150°C
Internal power dissipation		700mW
Lead temperature (soldering, 1,6 mm from case 10 seconds)		+260°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground terminal.

ELECTRICAL CHARACTERISTICS

At T_A = –40°C to +85°C, f_S = 40kSPS, V_S = 5V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER	TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
Resolution				16			16	Bits
ANALOG INPUT								
Voltage ranges			see Table 1			see Table 1		V
Impedance			see Table 1			see Table 1		Ω
Capacitance			45			45		pF
THROUGHPUT SPEED								
Conversion time	Acquire and convert			20			20	µs
Complete cycle	Acquire and convert			25			25	µs
Throughput rate	Acquire and convert	40			40			kSPS

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, f_S = 40kSPS, V_S = 5V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DC ACCURACY									
INL	Integral linearity error		–3		3	–2		2	LSB(1)
DNL	Differential linearity error		–2		3	–1		2	LSB
	No missing codes		15			16			Bits
	Transition noise(2)			0.6			0.6		LSB
	Full-scale error(3)(4)		–0.5		0.5	–0.25		0.25	%
	Full-scale error drift			10			10		ppm/°C
	Full-scale error(3)(4)	External 2.5V reference	–0.5		0.5	–0.25		0.25	%
	Full-scale error drift	External 2.5V reference		0.2			0.2		ppm/°C
	Bipolar zero error(3)	Bipolar ranges	–10		10	–10		10	mV
	Bipolar zero error drift	Bipolar ranges		2.5			2.5		ppm/°C
	Unipolar zero error(3)	Unipolar ranges	–6		6	–6		6	mV
	Unipolar zero error drift	Unipolar ranges		2.5			2.5		ppm/°C
	Recovery time to rated accuracy from power down(5)	1µF capacitor to CAP		300			300		µs
	Power-supply sensitivity	+4.75V < V_S < +5.25V			±8			±8	LSB
AC ACCURACY									
SFDR	Spurious-free dynamic range	f_{IN} = 1kHz, ±10V	90	100		96	102		dB(6)
THD	Total harmonic distortion	f_{IN} = 1kHz, ±10V		–98	–90		–100	–96	dB
SINAD	Signal-to-(noise+distortion)	f_{IN} = 1kHz, ±10V	85	89		87	89		dB
		-60 dB Input		30			32		
SNR	Signal-to-noise	f_{IN} = 1kHz, ±10V	85	89		87	89		dB
	Usable bandwidth(7)			130			130		kHz
	Full-power bandwidth (–3dB)			600			600		kHz
SAMPLING DYNAMICS									
	Aperture delay			40			40		ns
	Aperture jitter			20			20		ps
	Transient response	FS step		5			5		µs
	Overvoltage recovery(8)			750			750		ns
REFERENCE									
	Internal reference voltage	No load	2.48	2.5	2.52	2.48	2.5	2.52	V
	Internal reference source current (must use external buffer)			1			1		µA
	Internal reference drift			8			8		ppm/°C
	External reference voltage range for specified linearity		2.3	2.5	2.7	2.3	2.5	2.7	V
	External reference current drain	External 2.5V ref			100			100	µA

(1) *LSB* means *Least Significant Bit*. 1 LSB for the ±10V input range is 305µV.
(2) Typical rms noise at worst case transitions.
(3) As measured with fixed resistors. Adjustable to zero with external potentiometer.
(4) Full-scale error is the worst case of –Full Scale or +Full Scale deviation from ideal first and last code transitions, divided by the full-scale range; includes the effect of offset error. Tested at –40°C to +85°C.
(5) Time delay after the ADS8513 is brought out of Power-Down mode until all internal settling occurs and the analog input is acquired to rated accuracy. A Convert command after this delay will yield accurate results.
(6) All specifications in dB are referred to a full-scale input.
(7) Usable bandwidth defined as full-scale input frequency at which Signal-to-(Noise + Distortion) degrades to 60dB.
(8) Recovers to specified performance after 2 x FS input overvoltage.

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ELECTRICAL CHARACTERISTICS (continued)

At T_A = –40°C to +85°C, f_S = 40kSPS, V_S = 5V, and using internal reference and fixed resistors, unless otherwise specified.

PARAMETER		TEST CONDITIONS	ADS8513I			ADS8513IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL INPUTS									
V_{IL}	Low-level input voltage		–0.3		+0.8	–0.3		+0.8	V
V_{IH}	High-level input voltage		2.0		V_D +0.3 V	2.0		V_D +0.3 V	V
I_{IL}	Low-level input current	V_{IL} = 0V			±10				µA
I_{IH}	High-level input current	V_{IH} = 5V			±10				µA
DIGITAL OUTPUTS									
	Data format			Serial			Serial		
	Data coding			Binary twos complement			Binary twos complement		
V_{OL}	Low-level output voltage	I_{SINK} = 1.6mA			0.4			0.4	V
V_{OH}	High-level output voltage	I_{SOURCE} = 500µA	4			4			V
	Leakage Current	High-Z state, V_{OUT} = 0V to V_S			±1			±1	µA
	Output capacitance	High-Z state			15			15	pF
DIGITAL TIMING									
	Bus access time	R_L = 3.3kΩ, C_L = 50pF			83			83	ns
	Bus relinquish time	R_L = 3.3kΩ, C_L = 10pF			83			83	ns
POWER SUPPLIES									
V_S	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
I_{DIG}	Digital current			0.6			0.6		mA
I_{ANA}	Analog current			4.2			4.2		mA
	Power dissipation	V_S = 5V, f_S = 40kSPS		24	32.5		24	32.5	mW
		PWRD and REFD high		50			50		µW
TEMPERATURE RANGE									
	Specified performance		–40		+85	–40		+85	°C
	Derated performance		–55		+125	–55		+125	°C
	Storage temperature		–65		+150	–65		+150	°C
θ_{JA}	Thermal resistance			46			46		°C/W

Table 1. Input Ranges

ANALOG INPUT RANGE	CONNECT $R1_{IN}$ TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE (kΩ)
±10V	V_{IN}	BUF	GND	45.7
0.3125V to 2.8125V	V_{IN}	V_{IN}	V_{IN}	> 10,000
±5V	GND	BUF	V_{IN}	26.7
0V to 10V	BUF	GND	V_{IN}	26.7
0V to 4V	BUF	V_{IN}	GND	21.3
±3.33V	V_{IN}	BUF	V_{IN}	21.3
0.5V to 4.5V	GND	V_{IN}	GND	21.3

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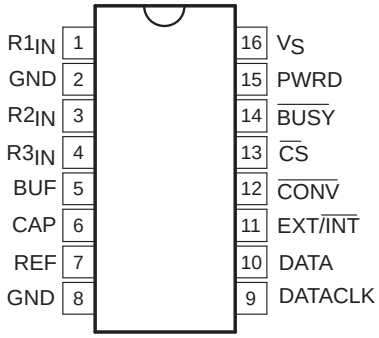
PIN CONFIGURATION

DW PACKAGE
SO-16
(TOP VIEW)



Pin Assignments

PIN		DIGITAL I/O	DESCRIPTION
NAME	NO.		
$R1_{IN}$	1		Analog input. See Table 1 and Table 3.
$R2_{IN}$	3		Analog input. See Table 1 and Table 3.
$R3_{IN}$	4		Analog input. See Table 1 and Table 3.
BUF	5		Reference buffer output. Connect to $R1_{IN}$, $R2_{IN}$, or $R3_{IN}$ as needed
CAP	6		Reference buffer compensation node. Decouple to ground with a 1-µF tantalum capacitor in parallel with a 0.01µF ceramic capacitor.
REF	7		Reference input/output. Outputs internal 2.5V reference via a series 4kΩ resistor. Decouple this voltage with a 1µF to 2.2µF tantalum capacitor to ground. If an external reference voltage is applied to this pin, it overrides the internal reference.
DATACLK	9	I/O	Data clock pin. With EXT/$\overline{INT}$ low, this pin is an output and provides the synchronous clock for the serial data. The output is 3-stated when $\overline{CS}$ is high. With EXT/$\overline{INT}$ high, this pin is an input and the serial data clock must be provided externally.
DATA	10	O	Serial data output. The serial data are always the result of the last completed conversion and are synchronized to DATACLK. If DATACLK is from the internal clock (EXT/$\overline{INT}$ low), the serial data are valid on both the rising and falling edges of DATACLK. DATA is 3-stated when $\overline{CS}$ is high.
EXT/$\overline{INT}$	11	I	External/Internal DATACLK pin. Selects the source of the synchronous clock for serial data. If high, the clock must be provided externally. If low, the clock is derived from the internal conversion clock. Note that the clock used to time the conversion is always interna,l regardless of the status of EXT/$\overline{INT}$.
$\overline{CONV}$	12		Convert input. A falling edge on this input puts the internal sample/hold into the hold state and starts a conversion regardless of the state of $\overline{CS}$. If a conversion is already in progress, the falling edge is ignored. If EXT/$\overline{INT}$ is low, data from the previous conversion are serially transmitted during the current conversion.
$\overline{CS}$	13	I	Chip select. This input 3-states all outputs when high and enables all outputs when low, including DATA, $\overline{BUSY}$, and DATACLK (when EXT/$\overline{INT}$ is low). Note that a falling edge on $\overline{CONV}$ initiates a conversion even when $\overline{CS}$ is high.
$\overline{BUSY}$	14	O	Busy output. When a conversion starts, $\overline{BUSY}$ goes low and remains low throughout the conversion. If EXT/$\overline{INT}$ is low, data are serially transmitted while $\overline{BUSY}$ is low. $\overline{BUSY}$ is 3-stated when $\overline{CS}$ is high.
PWRD	15	I	Power-down input. When high, the majority of the ADS8513 circuitry is placed in a low-power mode and power consumption is significantly reduced. (The ADS7813 requires $\overline{CONV}$ be taken low before PWRD goes low in order to achieve the lowest power consumption. This is not necessary for the ADS8513 and it does not cause interference if performed.) The time required for the ADS7813 to return to normal operation after power down depends on a number of factors. Consult the Chapter 0 section for more information.
GND	2, 8		Ground.
V_S	16		+5V supply input. For best performance, decouple to ground with a 0.1µF ceramic capacitor in parallel with a 10µF tantalum capacitor.

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TYPICAL CHARACTERISTICS

POWER-SUPPLY CURRENT vs FREE-AIR TEMPERATURE

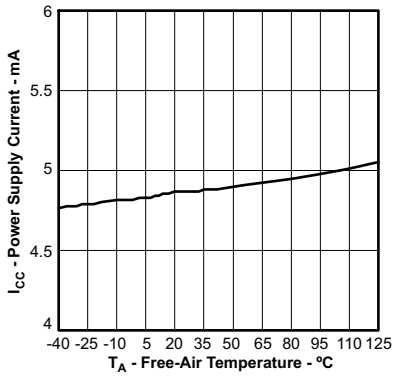

Figure 1.

INTERNAL REFERENCE VOLTAGE vs FREE-AIR TEMPERATURE

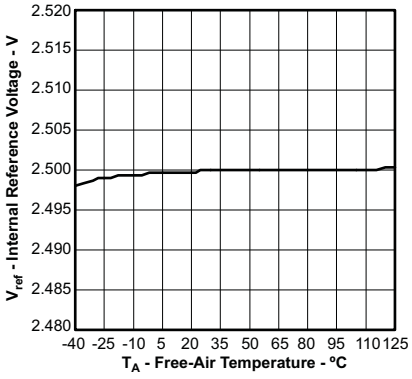

Figure 2.

POWER-SUPPLY CURRENT vs SAMPLING FREQUENCY

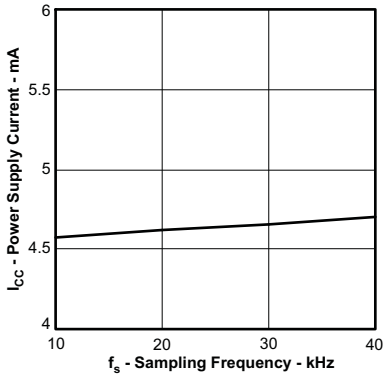

Figure 3.

BIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

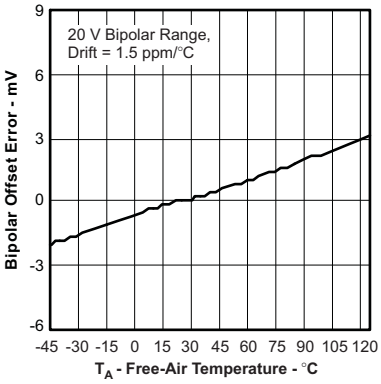

Figure 4.

BIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

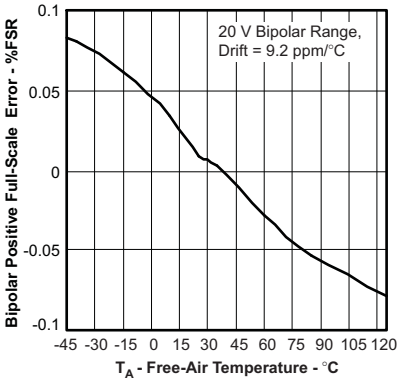

Figure 5.

BIPOLAR NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

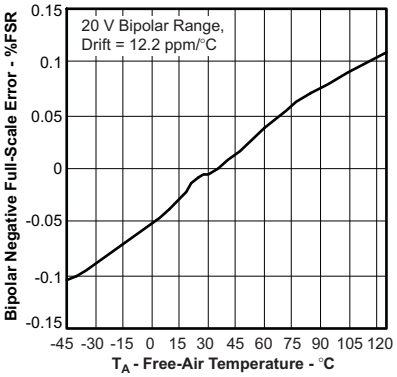

Figure 6.

BIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

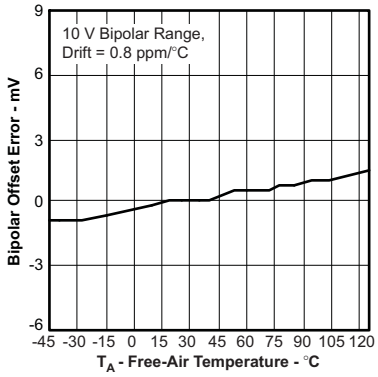

Figure 7.

BIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

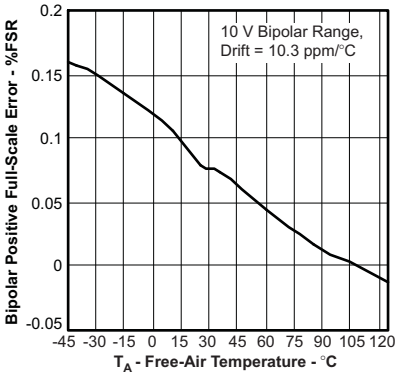

Figure 8.

BIPOLAR NEGATIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

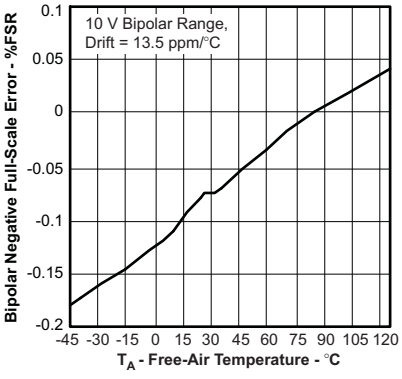

Figure 9.

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TYPICAL CHARACTERISTICS (continued)

UNIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

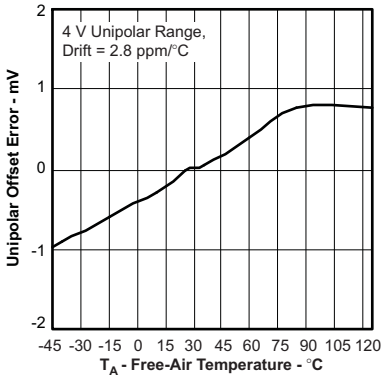

Figure 10.

UNIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

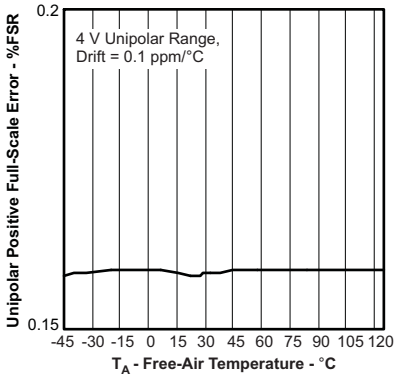

Figure 11.

UNIPOLAR OFFSET ERROR vs FREE-AIR TEMPERATURE

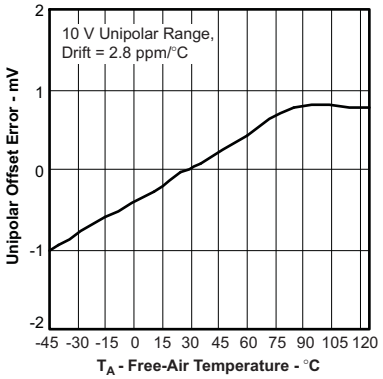

Figure 12.

UNIPOLAR POSITIVE FULL-SCALE ERROR vs FREE-AIR TEMPERATURE

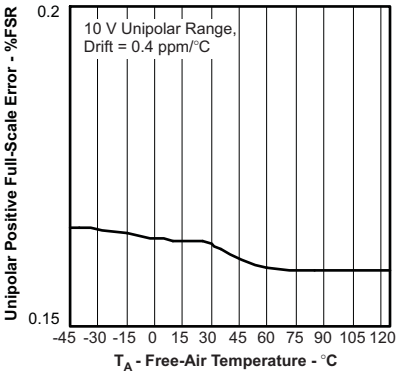

Figure 13.

SPURIOUS FREE DYNAMIC RANGE vs FREE-AIR TEMPERATURE

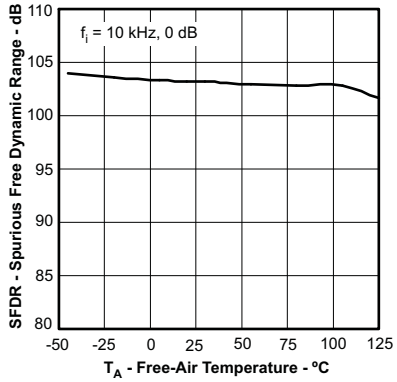

Figure 14.

TOTAL HARMONIC DISTORTION vs FREE-AIR TEMPERATURE

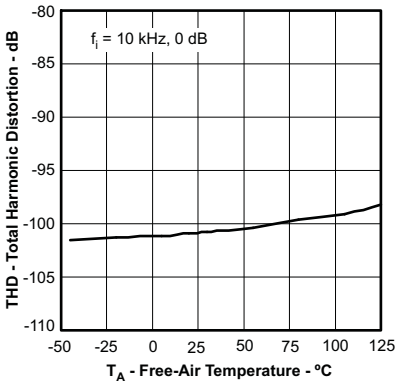

Figure 15.

SIGNAL-TO-NOISE RATIO vs FREE-AIR TEMPERATURE

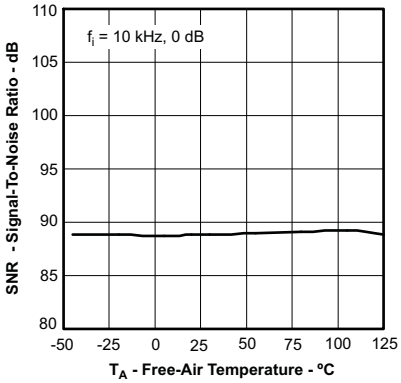

Figure 16.

SIGNAL-TO-NOISE + DISTORTION vs FREE-AIR TEMPERATURE

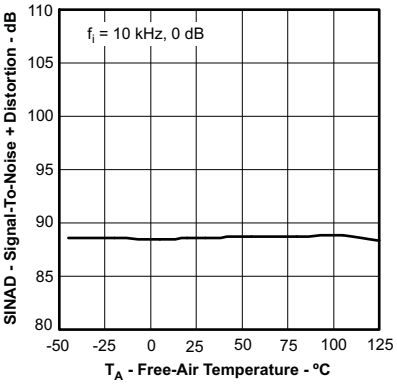

Figure 17.

SIGNAL-TO-NOISE + DISTORTION vs FREQUENCY

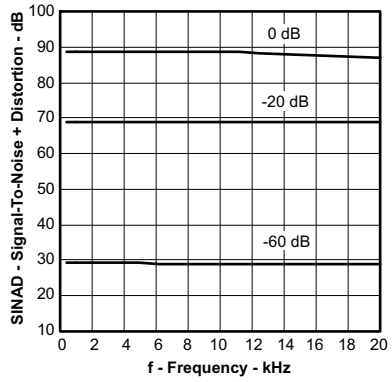

Figure 18.

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TYPICAL CHARACTERISTICS (continued)

SIGNAL-TO-NOISE + DISTORTION VS FREE-AIR TEMPERATURE

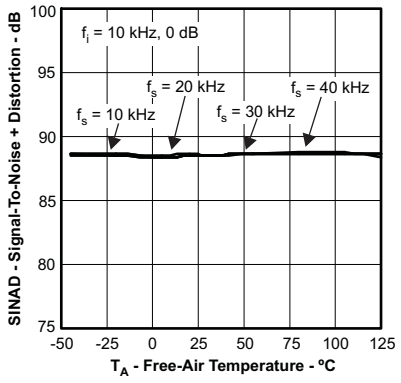

Figure 19.

SIGNAL-TO-NOISE RATIO VS FREQUENCY

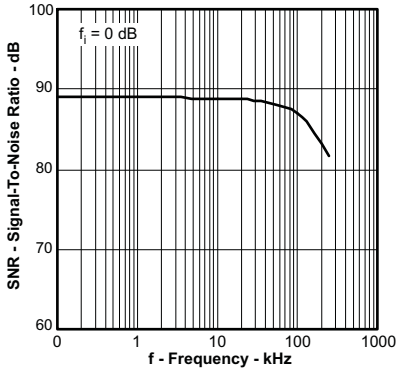

Figure 20.

SIGNAL-TO-NOISE + DISTORTION VS FREQUENCY

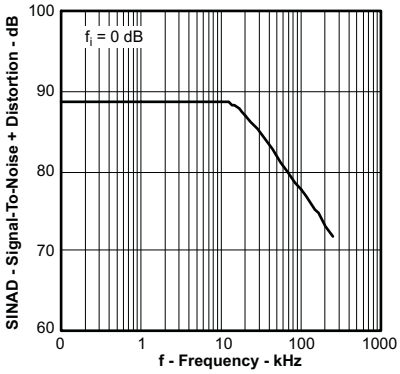

Figure 21.

SPURIOUS FREE DYNAMIC RANGE VS FREQUENCY

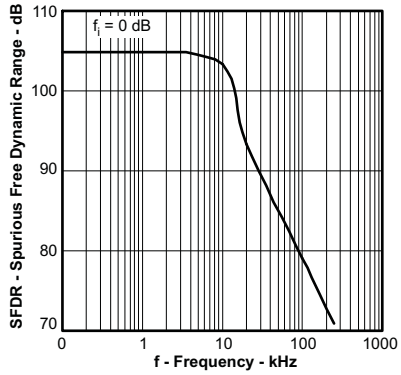

Figure 22.

TOTAL HARMONIC DISTORTION VS FREQUENCY

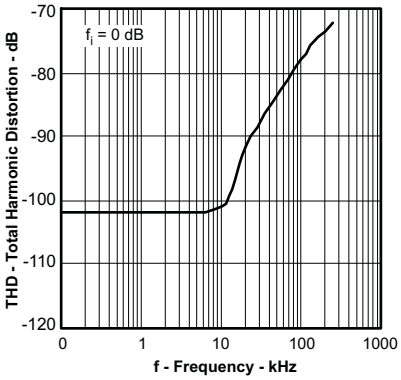

Figure 23.

SPURIOUS FREE DYNAMIC RANGE VS ESR

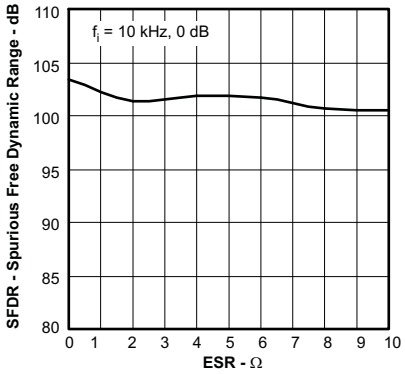

Figure 24.

TOTAL HARMONIC DISTORTION VS ESR

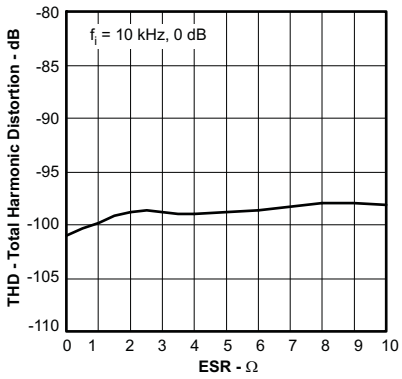

Figure 25.

SIGNAL-TO-NOISE RATIO VS ESR

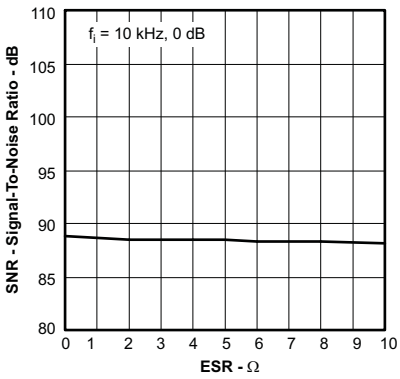

Figure 26.

SIGNAL-TO-NOISE + DISTORTION VS ESR

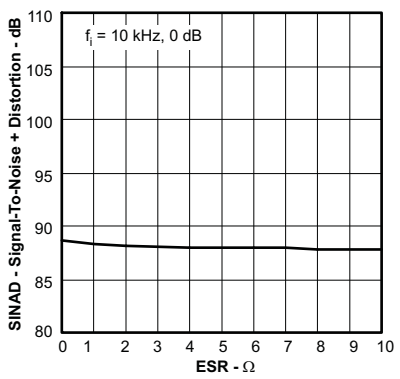

Figure 27.

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TYPICAL CHARACTERISTICS (continued)

CONVERSION TIME
vs
FREE-AIR TEMPERATURE

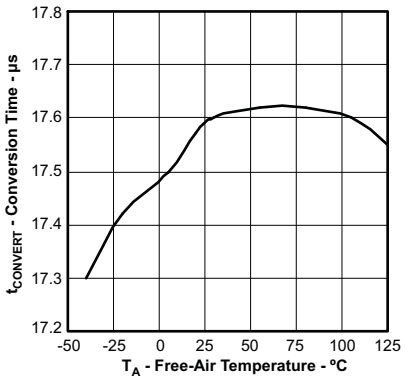

Figure 28.

OUTPUT REJECTION
vs
POWER-SUPPLY RIPPLE
FREQUENCY

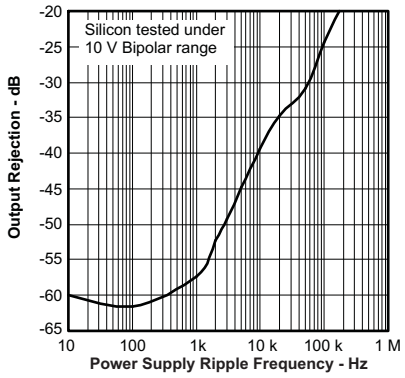

Figure 29.

INL

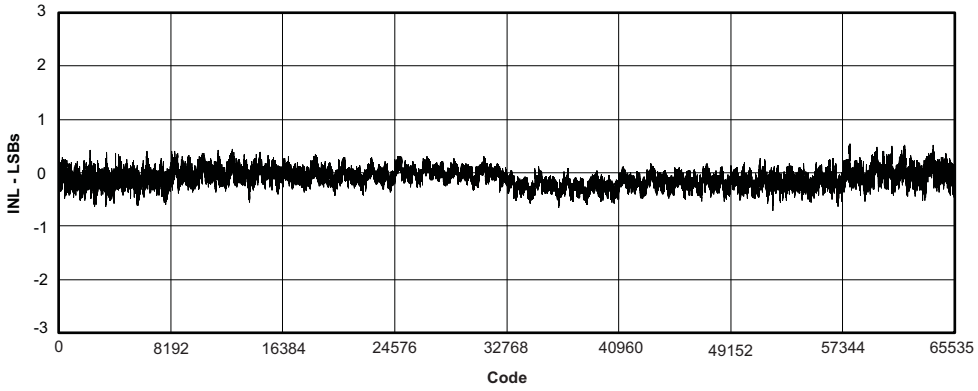

Figure 30.

DNL

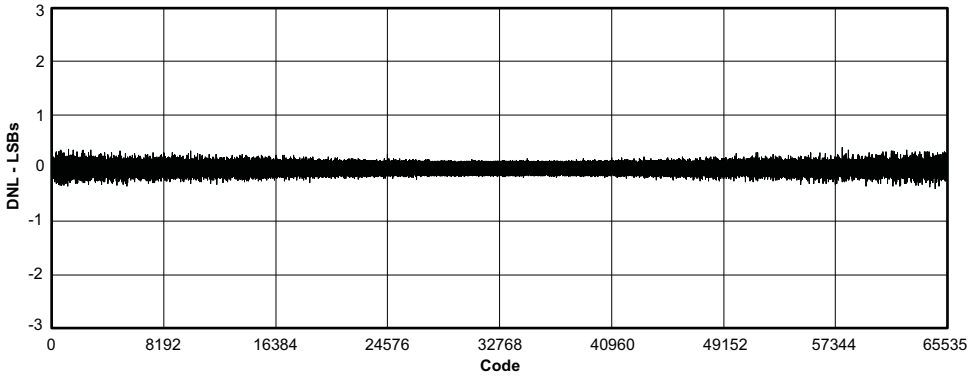

Figure 31.

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TYPICAL CHARACTERISTICS (continued)

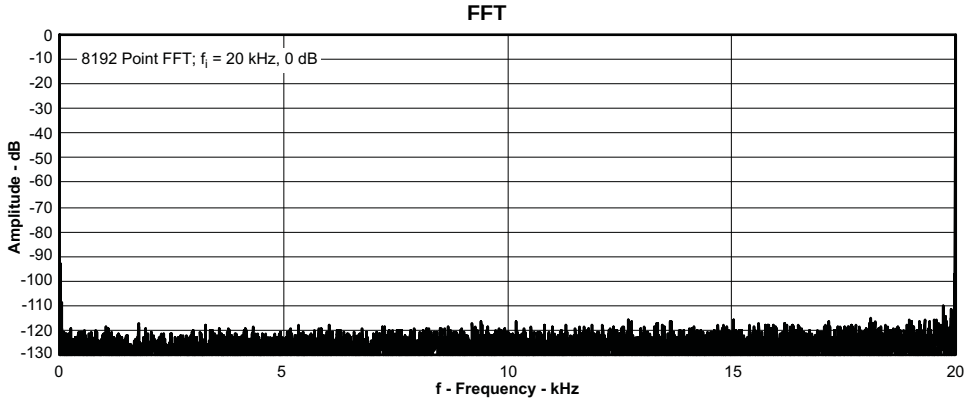

Figure 32.

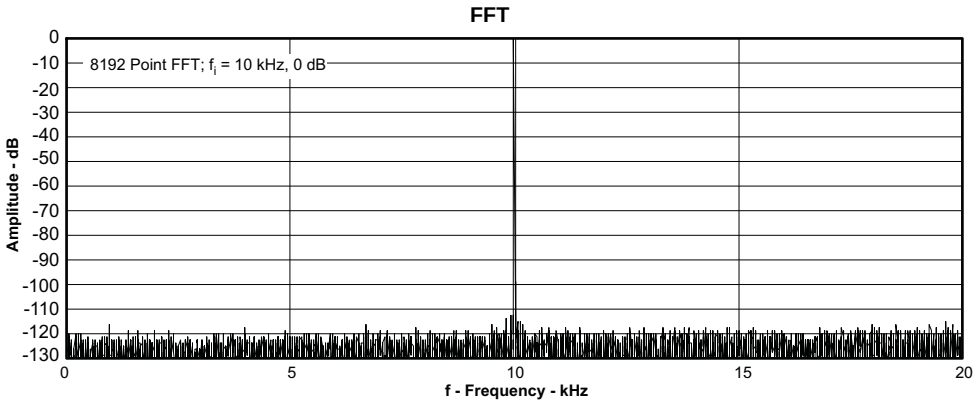

Figure 33.

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BASIC OPERATION

INTERNAL DATACLK

Figure 34 shows a basic circuit to operate the ADS8513 with a ±10V input range using an internal DATACLK. To begin a conversion and serial transmission of the results from the previous conversion, a falling edge must be provided to the CONV input. BUSY goes low to indicate that a conversion has started, and stays low until the conversion is complete. During the conversion, the results of the previous conversion are transmitted via DATA while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, binary twos complement, MSB first. Each data bit is valid on both the rising and falling edge of DATACLK. BUSY is low during the entire serial transmission and can be used as a frame synchronization signal.

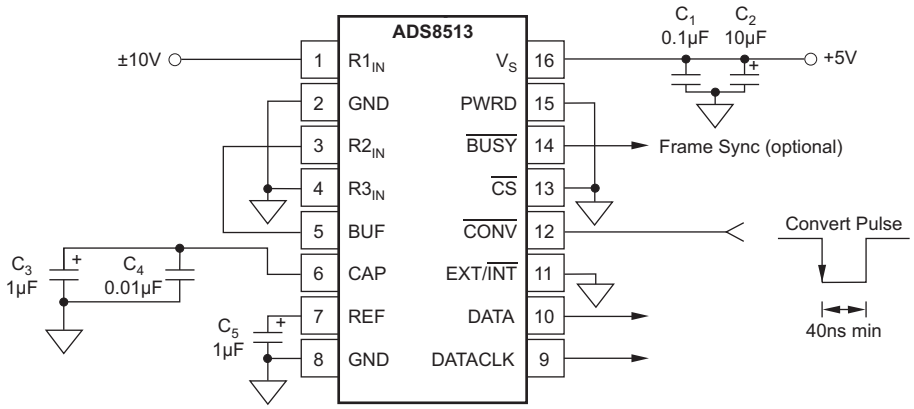
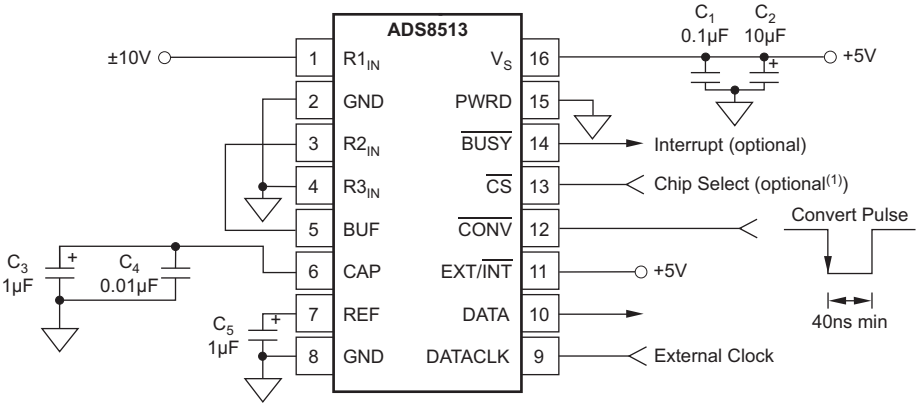


Figure 34. Basic Operating Circuit, ±10V Input Range, Internal DATACLK

EXTERNAL DATACLK

Figure 35 shows another basic circuit to operate the ADS8513 with a ±10V input rangeusing an external DATACLK. To begin a conversion, a falling edge must be provided to the CONV input. BUSY goes low to indicate that a conversion has started,and stays low until the conversion is complete. Just before BUSY rises near the end of the conversion, the conversion result held in the internal working register is transferred to the internal shift register.

The internal shift register is clocked via the DATACLK input. The recommended method of reading the conversion result is to provide the serial clock after the conversion has completed. See *External DATACLK* under the *Reading Data* section of this data sheet for more information.



NOTE: (1) Tie $\overline{CS}$ to GND if the outputs will always be active.

Figure 35. Basic Operating Circuit, ±10V Input Range, External DATACLK

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STARTING A CONVERSION

If a conversion is not currently in progress, a falling edge on the $\overline{CONV}$ input places the sample-and-hold into the hold mode and begins a conversion, as shown in Figure 36 according to the timing shown in Table 2. During the conversion, the $\overline{CONV}$ input is ignored. Starting a conversion does not depend on the state of $\overline{CS}$. A conversion can be started once every 25µs (40kSPS maximum conversion rate). There is no minimum conversion rate.

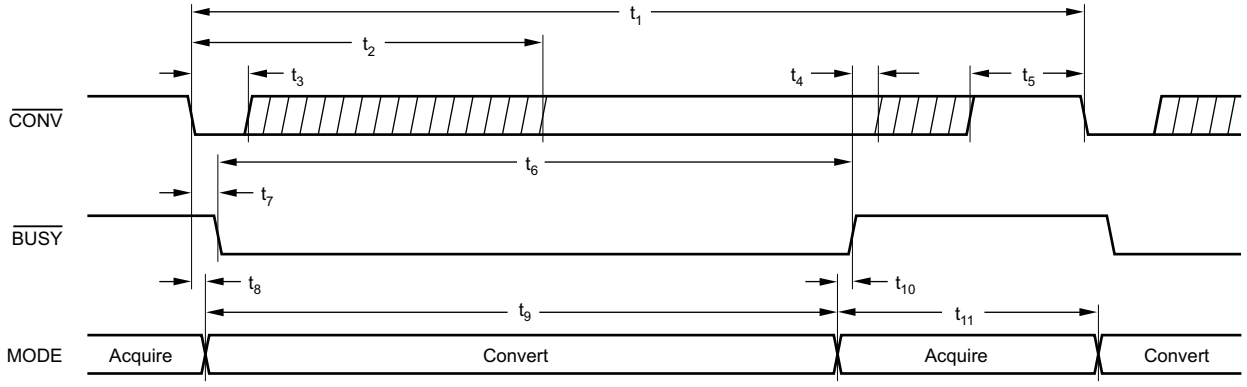

Figure 36. Basic Conversion Timing

Table 2. Conversion and Data Timing, T_A = –40°C to +85°C

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_1	Conversion plus acquisition time			25	µs
t_2	$\overline{CONV}$ low to all digital inputs stable			19	µs
t_3	$\overline{CONV}$ low to initiate a conversion	0.04		12	µs
t_4	$\overline{BUSY}$ rising to any digital input active	5			ns
t_5	$\overline{CONV}$ high prior to start of conversion ($\overline{CONV}$ high time)	15			ns
t_6	$\overline{BUSY}$ low		18	20	µs
t_7	$\overline{CONV}$ low to $\overline{BUSY}$ low		12	20	ns
t_8	Aperture delay ($\overline{CONV}$ falling edge to actual conversion start)		5		ns
t_9	Conversion time		18	20	µs
t_{10}	Conversion complete to $\overline{BUSY}$ rising		90		ns
t_{11}	Acquisition time		7		µs
t_{12}	$\overline{CONV}$ low to rising edge of first internal DATACLK		2.0		µs
t_{13}	Internal DATACLK high	300	410	425	ns
t_{14}	Internal DATACLK low	300	410	425	ns
t_{15}	Internal DATACLK period	0.6	0.82	0.85	µs
t_{16}	DATA valid to internal DATACLK rising	150	204		ns
t_{17}	Internal DATACLK falling to DATA not valid	150	208		ns
t_{18}	Falling edge of last DATACLK to $\overline{BUSY}$ rising		4.4	5	µs
t_{19}	External DATACLK rising to DATA not valid	4	14		ns
t_{20}	External DATACLK rising to DATA valid	2	12	20	ns
t_{21}	External DATACLK high	15			ns
t_{22}	External DATACLK low	15			ns
t_{23}	External DATACLK period	35			ns
t_{24}	$\overline{CONV}$ low to external DATACLK active	15			ns
t_{25}	External DATACLK low or $\overline{CS}$ high to $\overline{BUSY}$ rising			5	µs
t_{26}	$\overline{CS}$ low to digital outputs enabled	15			ns
t_{27}	$\overline{CS}$ high to digital outputs disabled	15			ns

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Even though the $\overline{\text{CONV}}$ input is ignored while a conversion is in progress, this input should be held static during the conversion period. Transitions on this digital input can easily couple into sensitive analog portions of the converter, adversely affecting the conversion results (see the *Sensitivity to External Digital Signals* section of this data sheet for more information).

Ideally, the $\overline{\text{CONV}}$ input should go low and remain low throughout the conversion. It should return high sometime after $\overline{\text{BUSY}}$ goes high. In addition, it should be high before the start of the next conversion for a minimum time period given by t_5. This period ensures that the digital transition on the $\overline{\text{CONV}}$ input does not affect the signal that is acquired for the next conversion.

An acceptable alternative is to return the $\overline{\text{CONV}}$ input high as soon after the start of the conversion as possible. For example, a negative-going pulse 100ns wide would make a good $\overline{\text{CONV}}$ input signal. It is strongly recommended that from time t_2 after the start of a conversion until $\overline{\text{BUSY}}$ rises, the $\overline{\text{CONV}}$ input should be held static (either high or low). During this time, the converter is more sensitive to external noise.

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READING DATA

The ADS8513 digital output is in Binary Two's Complement (BTC) format. Table 3 shows the relationship between the digital output word and the analog input voltage under ideal conditions.

Table 3. Output Codes and Ideal Input Voltages

DESCRIPTION	ANALOG INPUT RANGE		DIGITAL OUTPUT	
Full-scale range	±10V	0.5V to 4.5V	BINARY TWOS COMPLEMENT	
Least significant bit (LSB)	305µV	61µV	BINARY CODE	HEX CODE
+Full-scale (FS – 1LSB)	9.999695V	4.499939V	0111 1111 1111 1111	7FFF
Midscale	0V	2.5V	0000 0000 0000 0000	0000
One LSB below midscale	–305µV	2.499939µV	1111 1111 1111 1111	FFFF
–Full-scale	–10V	0.5V	1000 0000 0000 0000	8000

Figure 37 shows the relationship between the various digital inputs, digital outputs, and internal logic of the ADS8513. Figure 38 illustrates when the internal shift register of the ADS8513 is updated and how this update relates to a single conversion cycle. Together, these two figures define a very important aspect of the ADS8513: ***the conversion result is not available until after the conversion is complete***. The implications of this protocol are discussed in the following sections.

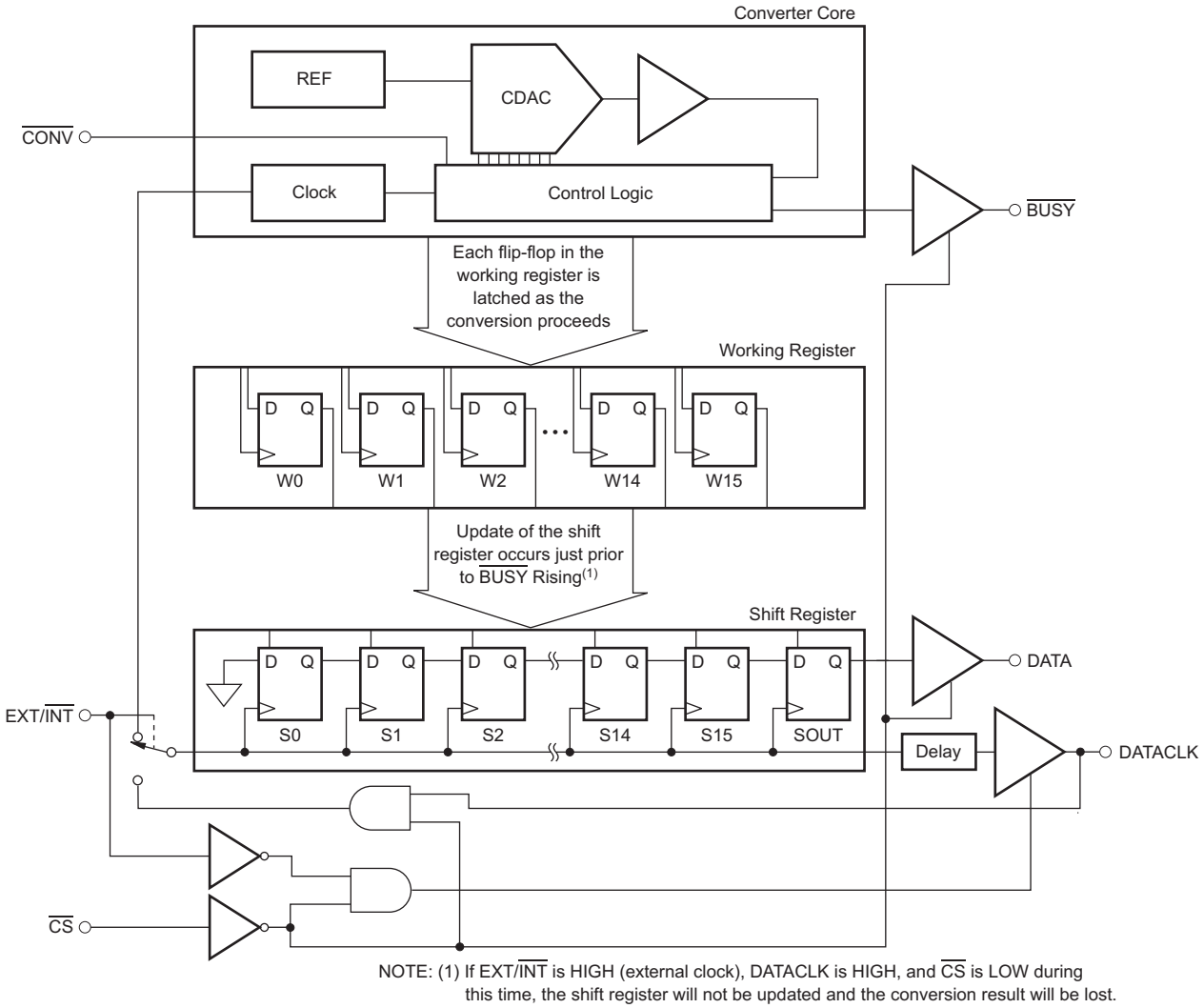

Figure 37. Block Diagram of the ADS8513 Digital Inputs and Outputs

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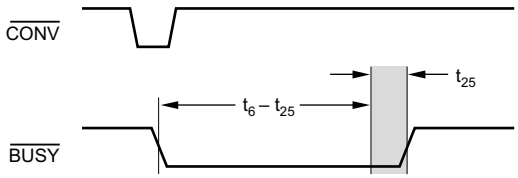

NOTE: Update of the internal shift register occurs in the shaded region. If EXT/$\overline{INT}$ is HIGH, then DATACLK must be LOW or $\overline{CS}$ must be HIGH during this time.

Figure 38. Shift Register Update Timing

INTERNAL DATACLK

With EXT/$\overline{INT}$ tied low, the result from conversion 'n' is serially transmitted during conversion 'n+1', as shown in Figure 39 and with the timing given in Table 2. Serial transmission of data occurs only during a conversion. When a transmission is not in progress, DATA and DATACLK are low.

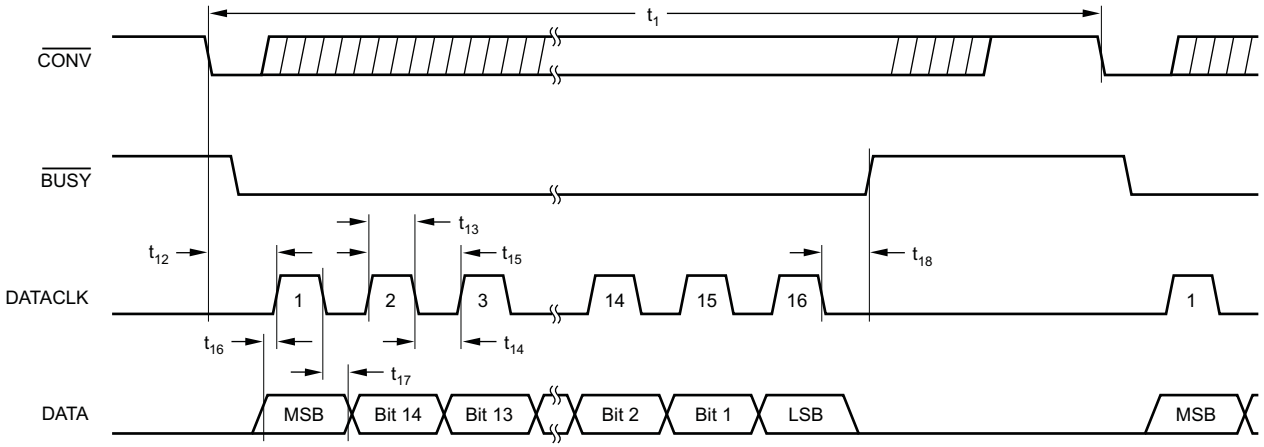

Figure 39. Serial Data Timing, Internal Clock (EXT/$\overline{INT}$ and $\overline{CS}$ Low)

During the conversion, the results of the previous conversion are transmitted via DATA, while DATACLK provides the synchronous clock for the serial data. The data format is 16-bit, Binary Two's Complement, MSB first. Each data bit is valid on both the rising and falling edges of DATACLK. $\overline{BUSY}$ is low during the entire serial transmission and can be used as a frame synchronization signal.

EXTERNAL DATACLK

With EXT/$\overline{INT}$ tied high, the result from conversion 'n' is clocked out after the conversion has completed, during the next conversion ('n+1'), or a combination of these two. Figure 40 shows the case of reading the conversion result after the conversion is complete. Figure 41 describes reading the result during the next conversion. Figure 42 combines the important aspects of Figure 40 and Figure 41 for reading part of the result after the conversion is complete and the balance during the next conversion.

The serial transmission of the conversion result is initiated by a rising edge on DATACLK. The data format is 16-bit, Binary Two's Complement, MSB first. Each data bit is valid on the falling edge of DATACLK. In some cases, it might be possible to use the rising edge of the DATACLK signal. However, one extra clock period (not shown in Figure 40, Figure 41, and Figure 42) is needed for the final bit.

The external DATACLK signal must be low or $\overline{CS}$ must be high before $\overline{BUSY}$ rises (see time t_{25} in Figure 41 and Figure 42). If this limit is not observed during this time, the output shift register of the ADS8513 is not updated with the conversion result. Instead, the previous contents of the shift register remain and the new result is lost.

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Before reading the next three paragraphs, consult the *Sensitivity to External Digital Signals* section of this data sheet. This section explains many of the concerns regarding how and when to apply the external DATACLK signal.

External DATACLK Active After the Conversion

The preferred method of obtaining the conversion result is to provide the DATACLK signal after the conversion has been completed and before the next conversion starts, as shown in Figure 40. Note that the DATACLK signal should be static before the start of the next conversion. If this limit is not observed, the DATACLK signal could affect the acquired.

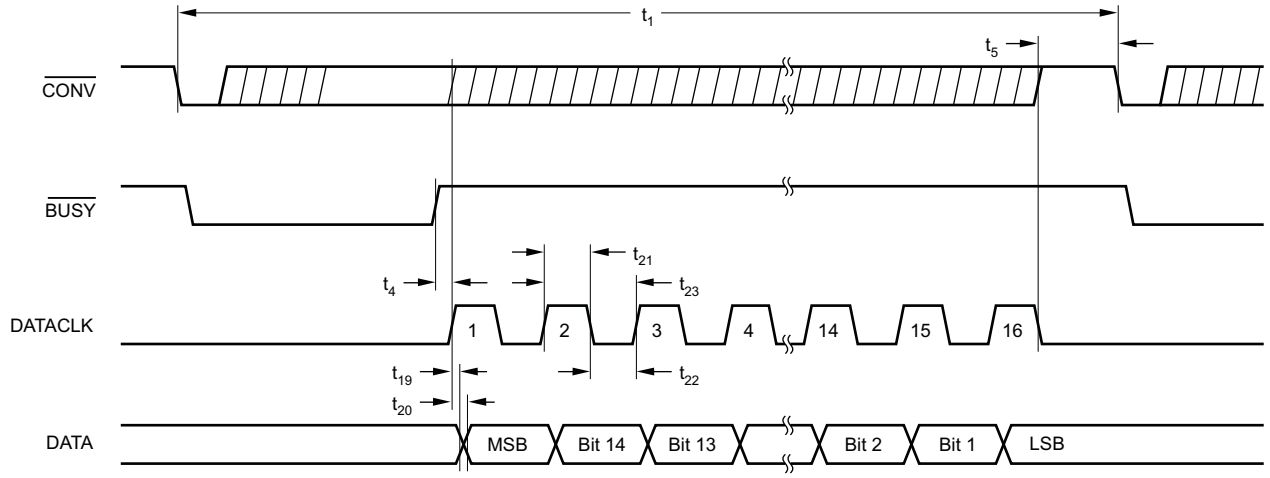

Figure 40. Serial Data Timing, External Clock, Clocking After the Conversion Completes (EXT/$\overline{INT}$ High, $\overline{CS}$ Low)

External DATACLK Active During the Next Conversion

Another method of obtaining the conversion result is shown in Figure 41. Because the output shift register is not updated until the end of the conversion, the previous result remains valid during the next conversion. If a fast clock (≥ 2MHz) can be provided to the ADS8513, the result can be read during time t_2. During this time, the noise from the DATACLK signal is less likely to affect the conversion result.

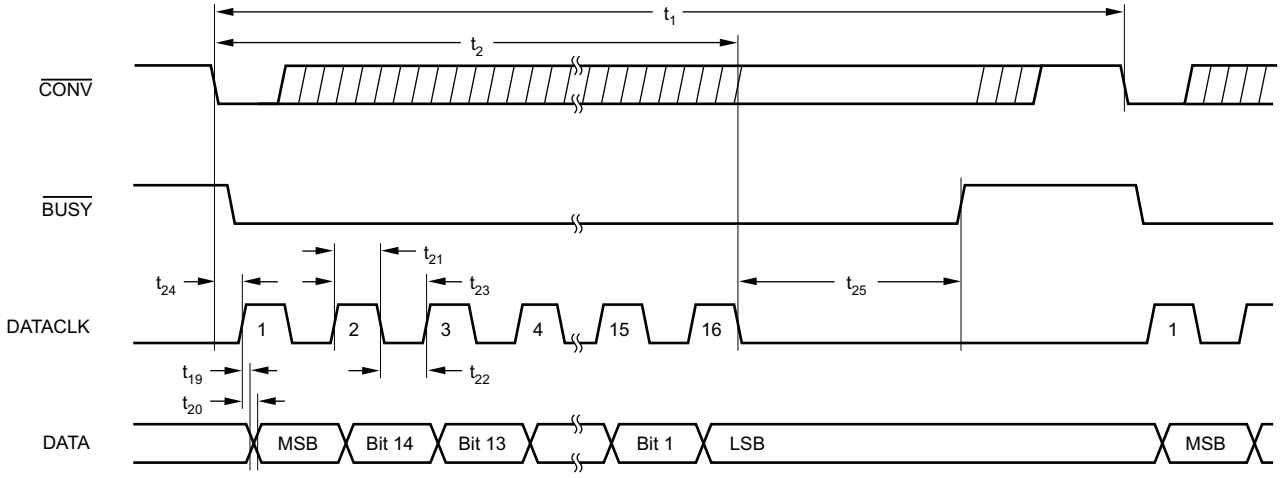

Figure 41. Serial Data Timing, External Clock, Clocking During the Next Conversion (EXT/$\overline{INT}$ High, $\overline{CS}$ Low)

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External DATACLK Active After the Conversion and During the Next Conversion

Figure 42 shows a method that combines the two previous approaches. This method works very well for microcontrollers that do serial transfers eight bits at a time and for slower microcontrollers. For example, if the fastest serial clock that the microcontroller can produce is 1µs, the approach shown in Figure 40 would result in a diminished throughput (26kSPS maximum conversion rate). The method described in Figure 41 could not be used without risk of affecting the conversion result (the clock would have to be active after time t_2). Therefore, the approach in Figure 42 results in an improved throughput rate (33kSPS maximum with a 1µs clock), and DATACLK is not active after time t_2.

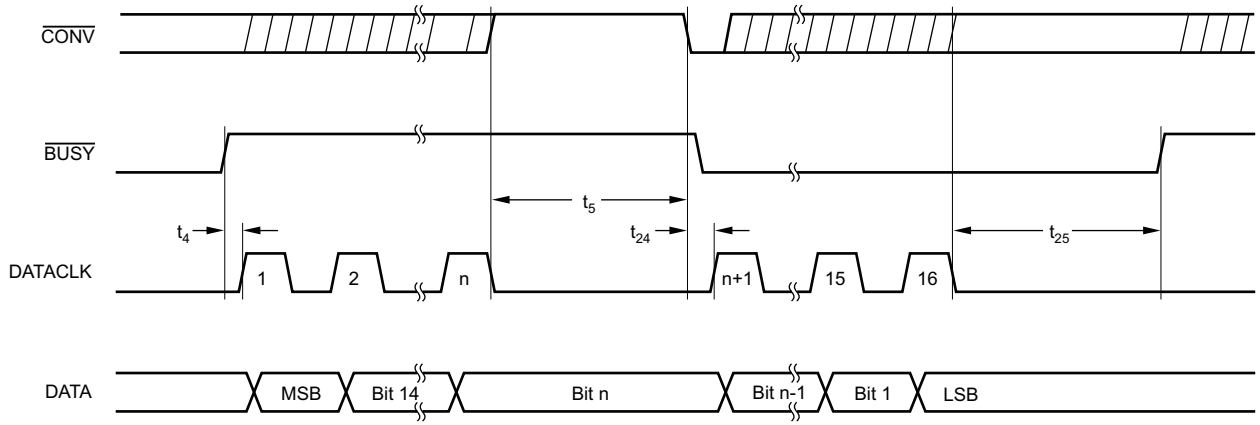
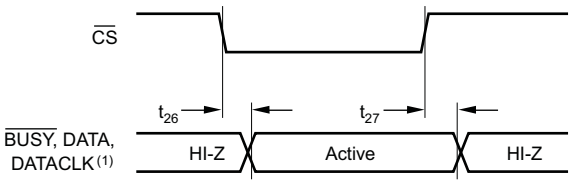


Figure 42. Serial Data Timing, External Clock, Clocking After the Conversion Completes and During the Next Conversion (EXT/INT High, CS Low)

CHIP SELECT

The CS input allows the digital outputs of the ADS8513 to be disabled and gates the external DATACLK signal when EXT/INT is high. See Figure 43 for the enable and disable time associated with CS and Figure 37 for a logic diagram of the ADS8513. The digital outputs can be disabled at any time.

Note that a conversion is initiated on the falling edge of CONV even if CS is high. If the EXT/INT input is low (internal DATACLK) and CS is high during the entire conversion, the previous conversion result is lost (that is, the serial transmission occurs but DATA and DATACLK are disabled).



NOTE: (1) DATACLK is an output only when EXT/INT is LOW.

Figure 43. Enable and Disable Timing for Digital Outputs

ANALOG INPUT

The ADS8513 offers a number of input ranges. This set of options is accomplished by connecting the three input resistors to either the analog input (V_{IN}), to ground (GND), or to the 2.5V reference buffer output (BUF). Table 1 shows the input ranges that are typically used in most data acquisition applications. These ranges are all specified to meet the specifications given in the *Electrical Characteristics* table. Table 4 contains a complete list of ideal input ranges, associated input connections, and comments regarding the range.

Table 4. Complete list of Ideal Input Ranges

ANALOG INPUT RANGE (V)	CONNECT $R1_{IN}$ TO	CONNECT $R2_{IN}$ TO	CONNECT $R3_{IN}$ TO	INPUT IMPEDANCE (kΩ)	COMMENT
0.3125 to 2.8125	V_{IN}	V_{IN}	V_{IN}	> 10,000	Specified offset and gain
–0.417 to 2.916	V_{IN}	V_{IN}	BUF	26.7	V_{IN} cannot go below GND – 0.3V
0.417 to 3.750	V_{IN}	V_{IN}	GND	26.7	Offset and gain not specified
±3.333	V_{IN}	BUF	V_{IN}	21.3	Specified offset and gain
–15 to 5	V_{IN}	BUF	BUF	45.7	Offset and gain not specified
±10	V_{IN}	BUF	GND	45.7	Specified offset and gain
0.833 to 7.5	V_{IN}	GND	V_{IN}	21.3	Offset and gain not specified
–2.5 to 17.5	V_{IN}	GND	BUF	45.7	Exceeds absolute maximum V_{IN}
2.5 to 22.5	V_{IN}	GND	GND	45.7	Exceeds absolute maximum V_{IN}
0 to 2.857	BUF	V_{IN}	V_{IN}	45.7	Offset and gain not specified
–1 to 3	BUF	V_{IN}	BUF	21.3	V_{IN} cannot go below GND – 0.3V
0 to 4	BUF	V_{IN}	GND	21.3	Specified offset and gain
–6.25 to 3.75	BUF	BUF	V_{IN}	26.7	Offset and gain not specified
0 to 10	BUF	GND	V_{IN}	26.7	Specified offset and gain
0.357 to 3.214	GND	V_{IN}	V_{IN}	45.7	Offset and gain not specified
–0.5 to 3.5	GND	V_{IN}	BUF	21.3	V_{IN} cannot go below GND – 0.3V
0.5 to 4.5	GND	V_{IN}	GND	21.3	Specified offset and gain
±5	GND	BUF	V_{IN}	26.7	Specified offset and gain
1.25 to 11.25	GND	GND	V_{IN}	26.7	Offset and gain not specified

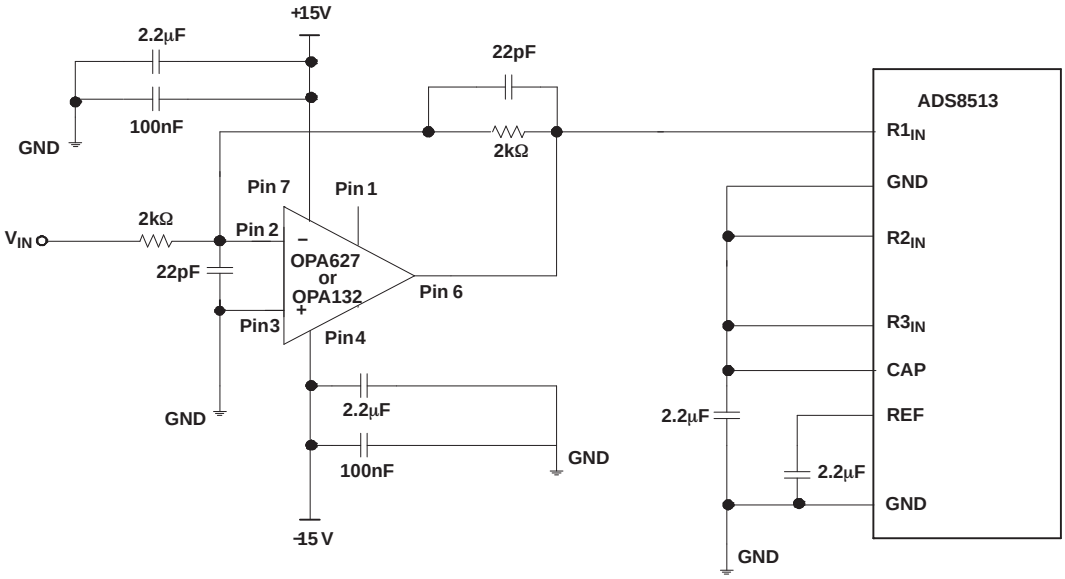


Figure 44. Typical Driving Circuit (±10V, No Trim)

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The input impedance results from the various connections and the internal resistor values (refer to the block diagram on the front page of this data sheet). The internal resistor values are typical and can change by ±30% as a result of process variations. However, the ratio matching of the resistors is considerably better than this range. Thus, the input range only varies a few tenths of a percent from part to part, while the input impedance can vary up to ±30%.

The Electrical Characteristics table contains the maximum limits for the variation of the analog input range, but only for those ranges where the comment field shows that the offset and gain are specified (including all the ranges listed in Table 1). For the other ranges, the offset and gain are not tested and are not specified.

Five of the input ranges in Table 4 are not recommended for general use. The upper-end of the –2.5V to +17.5V range and +2.5V to +22.5V range exceeds the absolute maximum analog input voltage. These ranges can still be used as long as the input voltage remains under the absolute maximum, but this limit may reduce the full-scale range of the converter to a significant degree.

Likewise, three of the input ranges involve the connection at $R2_{IN}$ being driven below GND. This input has a reverse-biased ESD protection diode connection to ground. If $R2_{IN}$ is taken below GND – 0.3V, this diode becomes forward-biased and clamps the negative input at –0.4V to –0.7V, depending on the temperature. Because the negative full-scale value of these input ranges exceeds –0.4V, they are not recommended.

Note that Table 4 assumes that the voltage at the REF pin is +2.5V. This assumption is true if the internal reference is used or if the external reference is +2.5V. Using other reference voltages change the values in Table 4.

HIGH IMPEDANCE MODE

When $R1_{IN}$, $R2_{IN}$, and $R3_{IN}$ are connected to the analog input, the input range of the ADS8513 is 0.3125V to 2.8125V and the input impedance is greater than 10MΩ. This input range can be used to connect the ADS8513 directly to a wide variety of sensors. Figure 45 shows the impedance of the sensor versus the change in integral linearity error (ILE) and differential linearity error (DLE) of the ADS8513. The performance of the ADS8513 can be improved for higher sensor impedance by allowing more time for acquisition. For example, 10µs of acquisition time approximately doubles the sensor impedance for the same ILE/DLE performance.

The input impedance and capacitance of the ADS8513 are very stable over temperature. Assuming that this performance is true of the sensor as well, the graph shown in Figure 45 will vary less than a few percent over the ensured temperature range of the ADS8513. If the sensor impedance varies significantly with temperature, the worst-case impedance should be used.

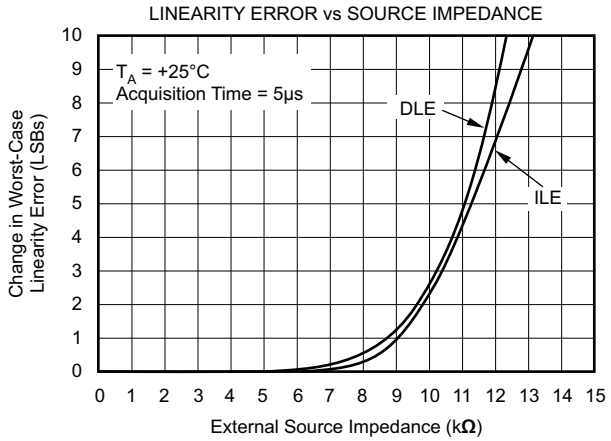

Figure 45. Linearity Error vs Source Impedance in the High Impedance Mode ($R1_{IN}$ = $R2_{IN}$ = $R3_{IN}$ = V_{IN})

DRIVING THE ADS8513 ANALOG INPUT

In general, any reasonably fast, high-quality operational or instrumentation amplifier can be used to drive the ADS8513 input. When the converter enters the acquisition mode, there is some charge injection from the converter input to the amplifier output. This charge injection can result in inadequate settling time with slower amplifiers. Be very careful with single-supply amplifiers, particularly if the output is required to swing very close to the supply rails.

In addition, be careful with regard to the amplifier linearity. The outputs of single-supply and rail-to-rail amplifiers can saturate as the outputs approach the supply rails. Rather than the amplifier transfer function being a straight line, the curve can become severely *S*-shaped. Also, watch for the point where the amplifier switches from sourcing current to sinking current. For some amplifiers, the transfer function can be noticeably discontinuous at this point, causing a significant change in the output voltage for a much smaller change on the input.

Texas Instruments manufactures a wide variety of operational and instrumentation amplifiers that can be used to drive the input of the ADS8513; these devices include the OPA627, OPA132, and INA110.

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REFERENCE

The ADS8513 can be operated with its internal 2.5V reference or an external reference. By applying an external reference voltage to the REF pin, the internal reference voltage is overdriven. The voltage at the REF input is internally buffered by a unity gain buffer. The output of this buffer is present at the BUF and CAP pins.

REF

The REF pin is the output of the internal 2.5V reference or the input for an external reference. A 1µF to 2.2µF tantalum capacitor should be connected between this pin and ground. The capacitor should be placed as close to the ADS8513 as possible.

When using the internal reference, the REF pin should not be connected to any type of significant load. An external load causes a voltage drop across the internal 4kΩ resistor that is in series with the internal reference. Even a 40MΩ external load to ground causes a decrease in the full-scale range of the converter by 6LSBs.

The range for the external reference is 2.3V to 2.7V. The voltage on REF determines the full-scale range of the converter and the corresponding LSB size. Increasing the reference voltage increases the LSB size in relation to the internal noise sources which, in turn, can improve signal-to-noise ratio. Likewise, decreasing the reference voltage reduces the LSB size and signal-to-noise ratio.

CAP

The ADS8513 is factory-tested with 2.2µF capacitors connected to pin 6 (CAP) and pin 7 (REF). Each capacitor should be placed as close as possible to its pin. The capacitor on pin 7 band-limits the internal reference noise. A lower-value capacitor can be used, but it may degrade SNR and SINAD. The capacitor on pin 6 stabilizes the reference buffer and provides a switching charge to the CDAC during conversion. Capacitors smaller than 1µF can cause the buffer to become unstable and may not hold sufficient charge for the CDAC. The parts are tested to specifications with 2.2µF, so larger capacitors are not necessary. The equivalent series resistance (ESR) of these compensation capacitors is also critical. The total ESR must be kept under 3Ω. See the *Typical Characteristics* section concerning how ESR affects performance.

BUF

The voltage on the BUF pin is the output of the internal reference buffer. This pin is used to provide +2.5V to the analog input or inputs for the various input configurations. The BUF output can provide up to 1mA of current to an external load. The load should be constant because variable load could affect the conversion result by modulating the BUF voltage. Also note that the BUF output shows significant glitches as each bit decision is made during a conversion. Between conversions, the BUF output is quiet.

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POWER DOWN

The ADS8513 has a power-down mode that is activated by taking $\overline{CONV}$ low and then PWRD high. This mode powers down all of the analog circuitry including the reference, reducing power dissipation to under 50µW. To exit the power-down mode, $\overline{CONV}$ is taken high and then PWRD is taken low. Note that a conversion is initiated if PWRD is taken high while $\overline{CONV}$ is low.

While in the power-down mode, the voltage on the capacitors connected to CAP and REF begins to leak off. The voltage on the CAP capacitor leaks off much more rapidly than on the REF capacitor (the REF input of the ADS8513 becomes high-impedance when PWRD is high; this condition is not true for the CAP input). When exiting power-down mode, these capacitors must be allowed to recharge and settle to a 16-bit level. Figure 46 shows the amount of time typically required to obtain a valid 16-bit result based on the amount of time spent in power down (at room temperature). This figure assumes that the total capacitance on the CAP pin is 1.01µF.

Figure 47 shows a circuit that can significantly reduce the power-up time if the power-down time is fairly brief (a few seconds or less). A low on-resistance MOSFET is used to disconnect the capacitance on the CAP pin from the leakage paths internal to the ADS8513. This MOSFET allows the capacitors to retain the respective charges for a much longer period of time, reducing the time required to recharge them at power-up. With this circuit, the power-down time can be extended to tens or hundreds of milliseconds with almost instantaneous power-up.

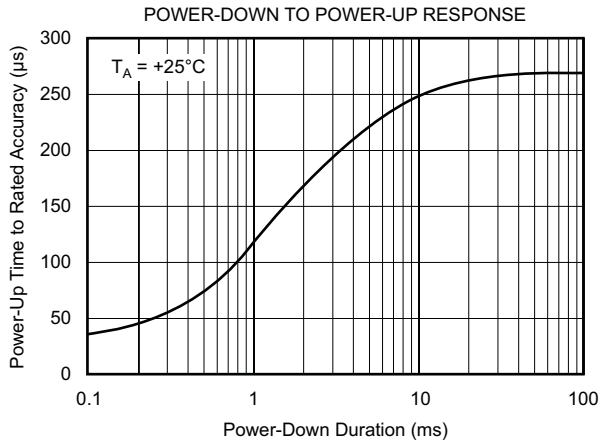

Figure 46. Power-Down to Power-Up Response

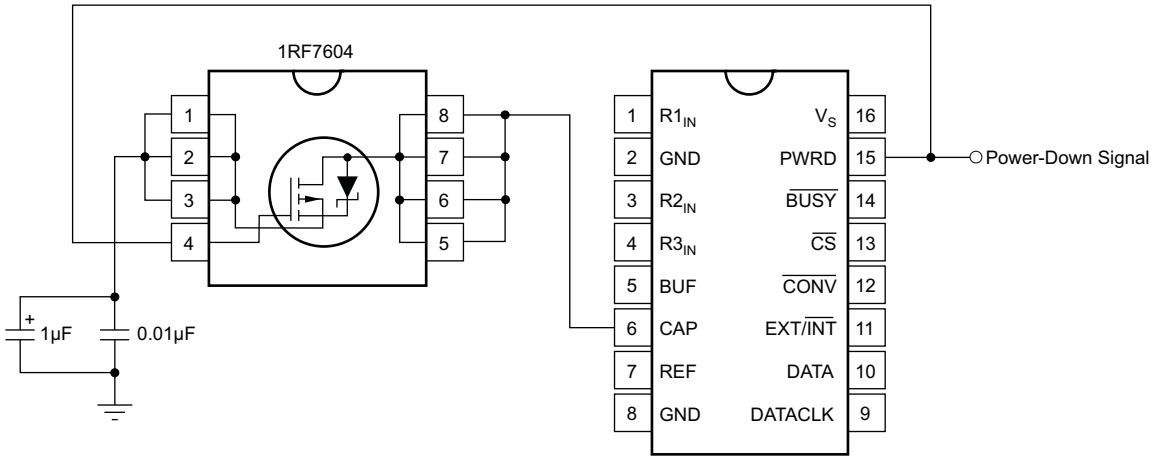

Figure 47. Improved Power-Up Response Circuit

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LAYOUT

POWER FOR TSSOP-20 PACKAGE

For optimum performance, tie the analog and digital power pins to the same +5V power supply and tie the analog and digital grounds together. As noted in the Electrical Characteristics table, the ADS8513 uses 90% of its power for the analog circuitry. The ADS8513 should be considered as an analog component.

The +5V power for the A/D converter should be separate from the +5V used for the system digital logic. Connecting $+V_{BD}$ directly to a digital supply can reduce converter performance because of switching noise from the digital logic. For best performance, the +5V supply can be produced from whatever analog supply is used for the rest of the analog signal conditioning. If +12V or +15V supplies are present, a simple +5V regulator can be used. Although it is not suggested, if the digital supply must be used to power the converter, be sure to properly filter the supply. Either using a filtered digital supply or a regulated analog supply, both $+V_{BD}$ and $+V_A$ should be tied to the same +5V source.

GROUNDING

All of the ground pins of the A/D converter should be tied to an analog ground plane, separated from the system digital logic ground to achieve optimum performance. Both analog and digital ground planes should be tied to the *system* ground as close to the power supplies as possible. This layout helps to prevent dynamic digital ground currents from modulating the analog ground through a common impedance to power ground.

SIGNAL CONDITIONING

The FET switches used for the sample-and-hold on many CMOS A/D converters release a significant amount of charge injection that can cause the driving op amp to oscillate. The amount of charge injection that results from the sampling FET switch on the ADS8513 is approximately 5% to 10% of the amount on similar A/D converters with the charge redistribution digital-to-analog converter (DAC) CDAC architecture. There is also a resistive front-end that attenuates any charge which is released. The end result is a minimal requirement for the drive capability on the signal conditioning preceding the A/D converter. Any op amp sufficient for the signal in an application is sufficient to drive the ADS8513.

The resistive front-end of the ADS8513 also provides a specified ±25V overvoltage protection. In most cases, this architecture eliminates the need for external over-voltage protection circuitry.

SENSITIVITY TO EXTERNAL DIGITAL SIGNALS

All successive approximation register-based A/D converters are sensitive to external noise sources. For the ADS8513 and similar A/D converters, this noise most often originates because of the transition of external digital signals. While digital signals that run near the converter can be the source of the noise, the biggest problem occurs with the digital inputs to the converter itself.

In many cases, the system designer may not be aware that there is a problem or the potential for a problem. For a 12-bit system, these problems typically occur at the least significant bits and only at certain places in the converter transfer function. For a 16-bit converter, the problem can be much easier to spot.

For example, the timing diagram in Figure 36 shows that the $\overline{\text{CONV}}$ signal should return high sometime during time t_2. In fact, the $\overline{\text{CONV}}$ signal can return high at any time during the conversion. However, after time t_2, the transition of the $\overline{\text{CONV}}$ signal has the potential of creating a good deal of noise on the ADS8513 die. If this transition occurs at just precisely the wrong time, the conversion results could be affected. In a similar manner, transitions on the DATACLK input could affect the conversion result.

For the ADS8513, there are 16 separate bit decisions that are made during the conversion. The most significant bit decision is made first, proceeding to the least significant bit at the end of the conversion. Each bit decision involves the assumption that the bit being tested should be set. This action is combined with the result that has been achieved so far. The converter compares this combined result with the actual input voltage. If the combined result is too high, the bit is cleared. If the result is equal to or lower than the actual input voltage, the bit remains high. This effect is why the basic architecture is referred to as a *successive approximation register* (SAR).

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If the result so far is getting very close to the actual input voltage, then the comparison involves two voltages that are very close together. The ADS8513 has been designed so that the internal noise sources are at a minimum just before the comparator result is latched. However, if an external digital signal transitions at this time, a great deal of noise will be coupled into the sensitive analog section of the ADS8513. Even if this noise produces a difference between the two voltages of only 2mV, the conversion result will be off by 52 counts or least significant bits (LSBs). (The internal LSB size of the ADS8513 is 38μV, regardless of the input range.)

Once a digital transition has caused the comparator to make a wrong bit decision, the decision cannot be corrected (unless some type of error correction is employed). All subsequent bit decisions will then be wrong. Figure 48 shows a successive approximation process that has gone wrong. The dashed line represents what the correct bit decisions should have been. The solid line represents the actual result of the conversion.

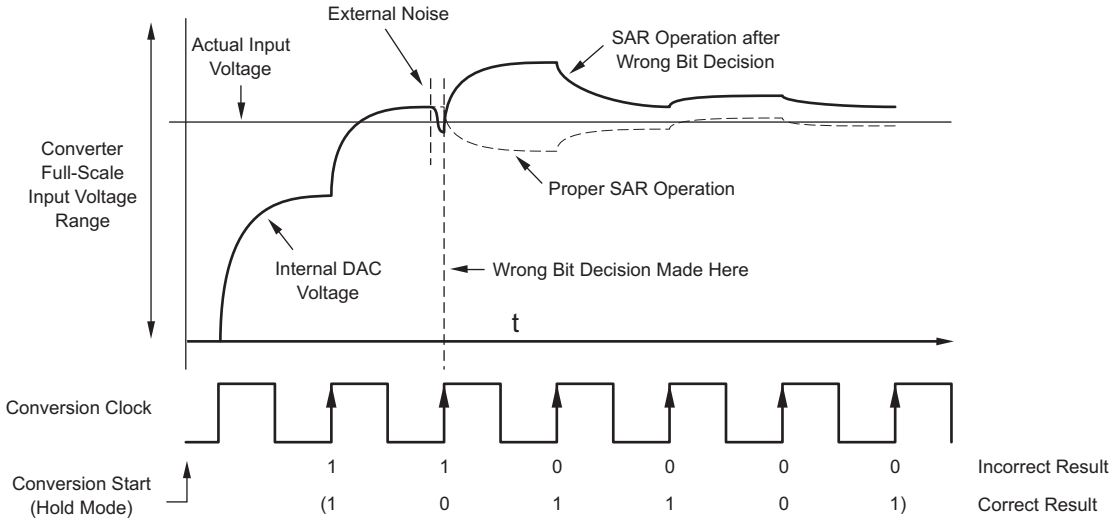

Figure 48. SAR Operation When External Noise Affects the Conversion

Keep in mind that the time period when the comparator is most sensitive to noise is fairly small. Also, the peak portion of the noise event produced by a digital transition is fairly brief, because most digital signals transition in a few nanoseconds. The subsequent noise may last for a period of time longer than this and may induce further effects that require a longer settling time. However, in general, the event is over within a few tens of nanoseconds.

For the ADS8513, error correction is done when the tenth bit is decided. During this bit decision, it is possible to correct limited errors that may have occurred during previous bit decisions. However, after the tenth bit, no such correction is possible. Note that for the timing diagrams shown in Figure 36, Figure 39, Figure 40, Figure 41, and Figure 42, all external digital signals should remain static from 8μs after the start of a conversion until $\overline{\text{BUSY}}$ rises. The tenth bit is decided approximately 10μs to 11μs into the conversion.

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APPLICATION INFORMATION

TRANSITION NOISE

Apply a dc input to the ADS8513 and initiate 1000 conversions. The digital output of the converter varies in output codes because the internal noise of the ADS8513. This condition is true for all 16-bit SAR converters. The transition noise specification found in the Electrical Characteristics table is a statistical figure that represents the 1σ limit or rms value of these output codes.

Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal output code for the input voltage value. The ±1σ, ±2σ, and ±3σ distributions represent 68.3%, 95.5%, and 99.7% of all codes. Multiplying transition noise by 6 yields the ±3σ distribution, or 99.7% of all codes. Statistically, up to three codes could fall outside the five-code distribution when executing 1000 conversions. The ADS8513 has a transition noise of 0.8 LSBs which yields five output codes for a ±3σ distribution. Figure 49 shows 16,384 conversion histogram results.

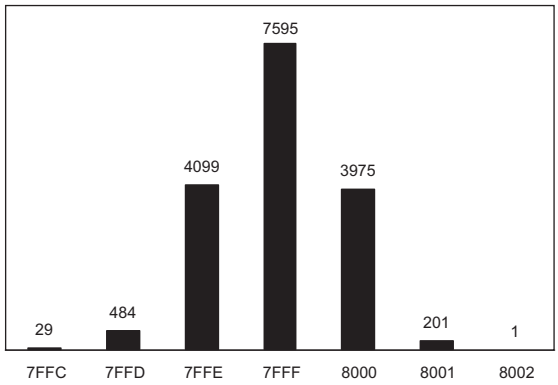

Figure 49. Histogram of 16384 Conversions With V_{IN} = 0V in ±10V Bipolar Range

AVERAGING

Converter noise can be compensated by averaging the digital codes. By averaging conversion results, transition noise is reduced by a factor of $1/\sqrt{n}$, where *n* is the number of averages. For example, averaging four conversion results reduces the transition noise by half to 0.4 LSBs. Note that averaging should only be used for input signals with frequencies near dc.

For ac signals, a digital filter can be used to low-pass filter and decimate the output codes. This action works in a similar manner to averaging: for every decimation by 2, the signal-to-noise ratio improves 3dB.

QSPI™ INTERFACE

Figure 50 shows a simple interface between the ADS8513 and any QSPI-equipped microcontroller. This interface assumes that the convert pulse does not originate from the microcontroller and that the ADS8513 is the only serial peripheral.

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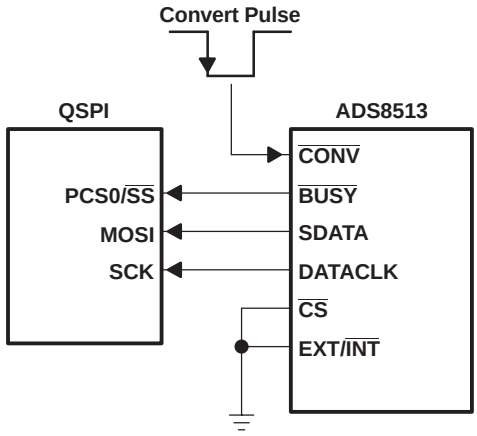

Figure 50. QSPI Interface to the ADS8513

Before enabling the QSPI interface, the microcontroller must be configured to monitor the slave select line. When a transition from high to low occurs on slave select (SS) from BUSY (indicating the end of the current conversion), the port can be enabled. If this enabling is not done, the microcontroller and the A/D converter may be *out-of-sync*.

Figure 51 shows another interface between the ADS8513 and a QSPI-equipped microcontroller that allows the microcontroller to give the convert pulses while also allowing multiple peripherals to be connected to the serial bus. This interface and the following discussion assume a master clock for the QSPI interface of 16.78MHz. Notice that the serial data input of the microcontroller is tied to the MSB (D7) of the ADS8513 instead of the serial output (SDATA). Using D7 instead of the serial port offers 3-state capability that allows other peripherals to be connected to the MISO pin. When communication is desired with those peripherals, PCS0 and PCS1 should be left high, which keeps D7 3-stated.

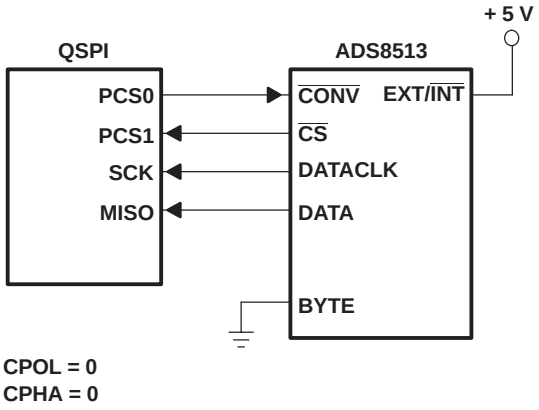

Figure 51. QSPI Interface to the ADS8513, Processor Initiates Conversions

In this configuration, the QSPI interface is actually set to do two different serial transfers. The first, an 8-bit transfer, causes PCS0 (CONV) and PCS1 (CS) to go low, starting a conversion. The second, a 16-bit transfer, causes only PCS1 (CS) to go low. This point is when the valid data are transferred.

For both transfers, the DT register (delay after transfer) is used to cause a 19µs delay. The interface is also set up to wrap to the beginning of the queue. In this manner, the QSPI is a state machine that generates the appropriate timing for the ADS8513. This timing is thus locked to the crystal-based timing of the microcontroller and not interrupt-driven. So, this interface is appropriate for both ac and dc measurements.

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For the fastest conversion rate, the baud rate should be set to 2 (4.19MHz SCK), DT set to 10, the first serial transfer set to 8 bits, the second set to 16 bits, and DSCK disabled (in the command control byte). This allows for a 23kSPS maximum conversion rate. For slower rates, DT should be increased. Do not slow SCK as this may increase the chance of affecting the conversion results or accidently initiating a second conversion during the first 8-bit transfer.

In addition, CPOL and CPHA should be set to zero (SCK normally low and data captured on the rising edge). The command control byte for the 8-bit transfer should be set to 20h and for the 16-bit transfer to 61h.

SPI INTERFACE

The SPI interface is generally only capable of 8-bit data transfers. For some microcontrollers with SPI interfaces, it might be possible to receive data in a similar manner as shown for the QSPI interface in Figure 50. The microcontroller must fetch the eight most significant bits before the contents are overwritten by the least significant bits.

A modified version of the QSPI interface shown in Figure 51 might be possible. For most microcontrollers with a SPI interface, the automatic generation of the start-of-conversion pulse is impossible and has to be done with software. This configuration limits the interface to dc applications because of the insufficient jitter performance of the convert pulse itself.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (August 2008) to Revision C **Page**

- Changed note 4 at the bottom of the Electrical Characteristics table 3

Changes from Revision A (March 2008) to Revision B **Page**

- Changed feature bullet for max power dissipation from 32.5W to 32.5mW 1
- Changed feature bullet for SPI serial port from 10Mhz to 20Mhz 1
- Changed Absolute Maximum Ratings to show actual device voltage and ground 2
- Changed Electrical Characteristics to show actual device voltage and ground 2

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS8513IBDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8513I B	Samples
ADS8513IBDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8513I B	Samples
ADS8513IDW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8513I	Samples
ADS8513IDWG4	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8513I	Samples
ADS8513IDWR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	ADS8513I	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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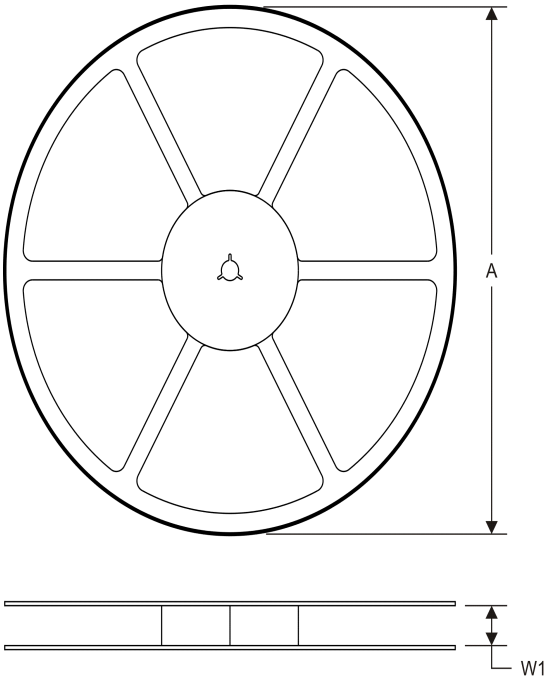
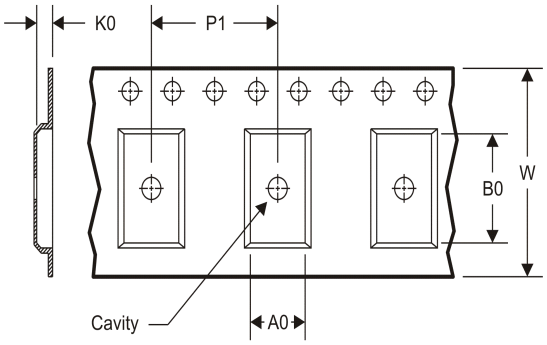
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



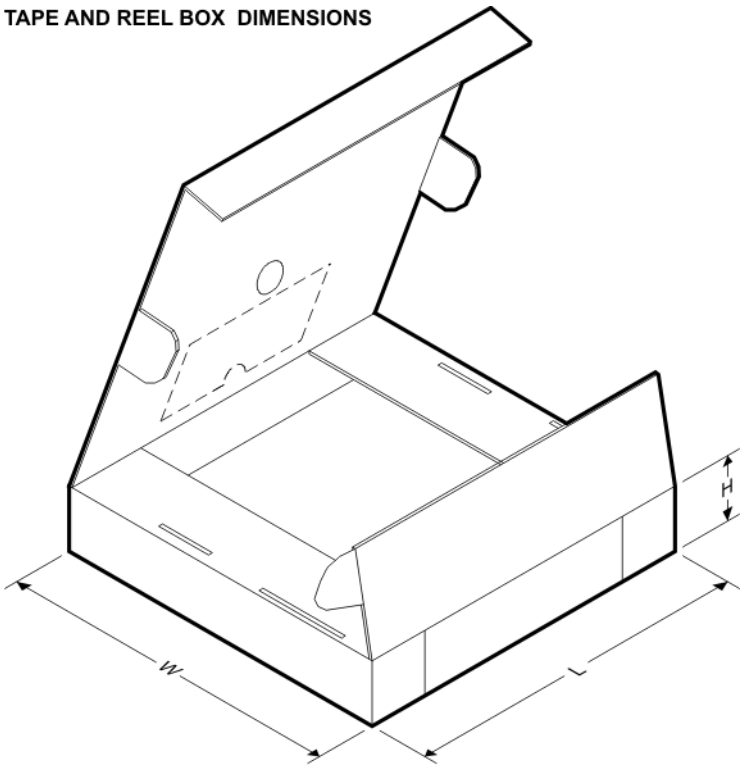
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8513IBDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
ADS8513IDWR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



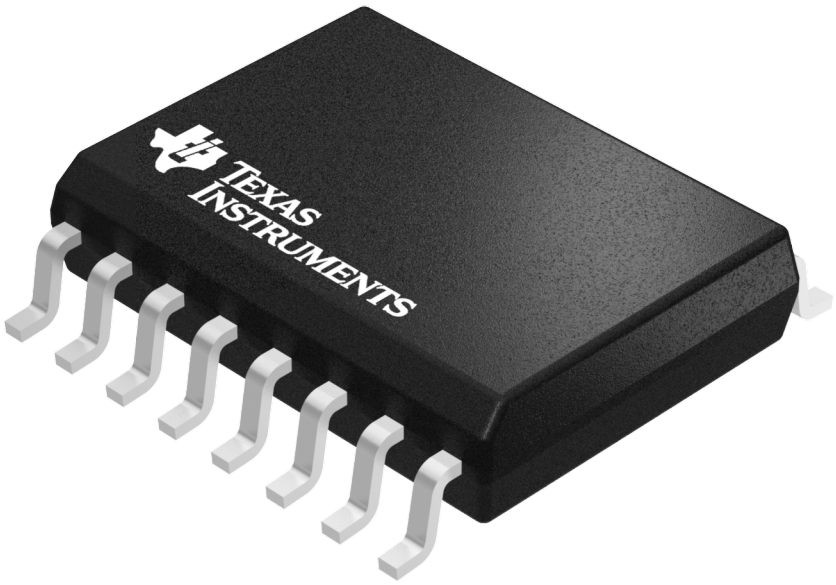
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8513IBDWR	SOIC	DW	16	2000	367.0	367.0	38.0
ADS8513IDWR	SOIC	DW	16	2000	367.0	367.0	38.0

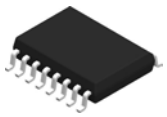
GENERIC PACKAGE VIEW

DW 16 SOIC - 2.65 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

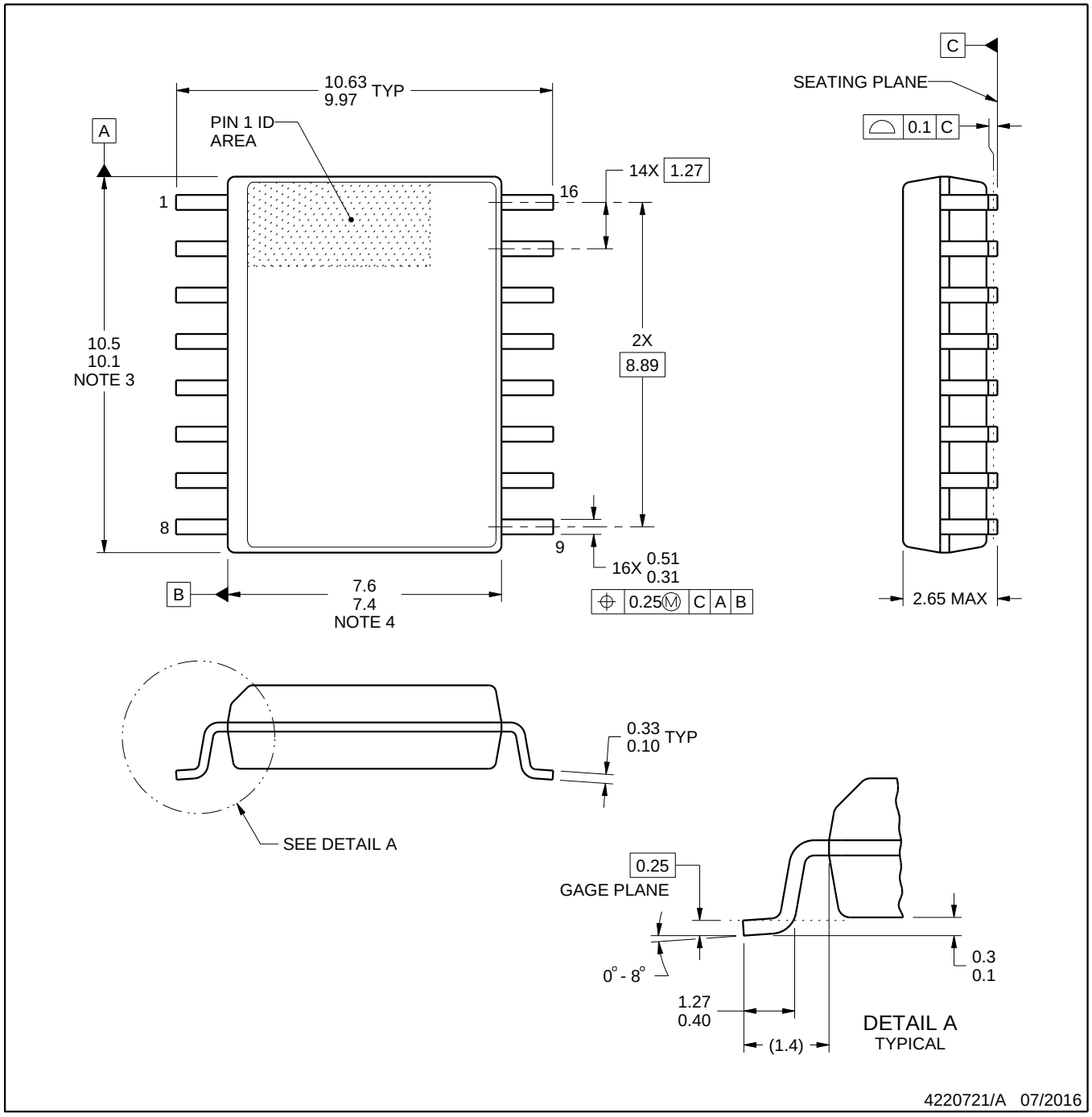


PACKAGE OUTLINE

DW0016A

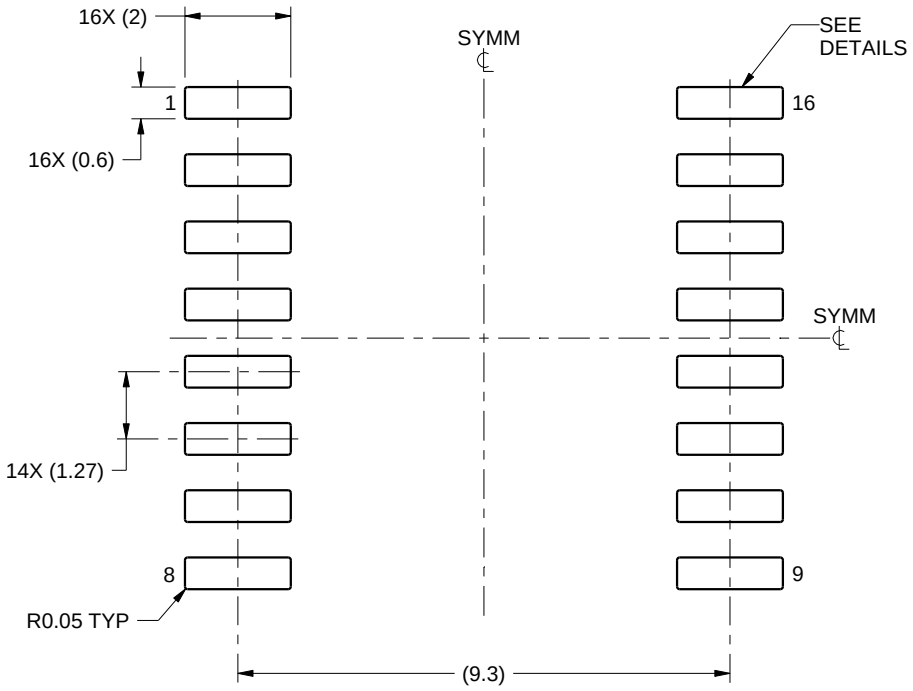
SOIC - 2.65 mm max height

SOIC

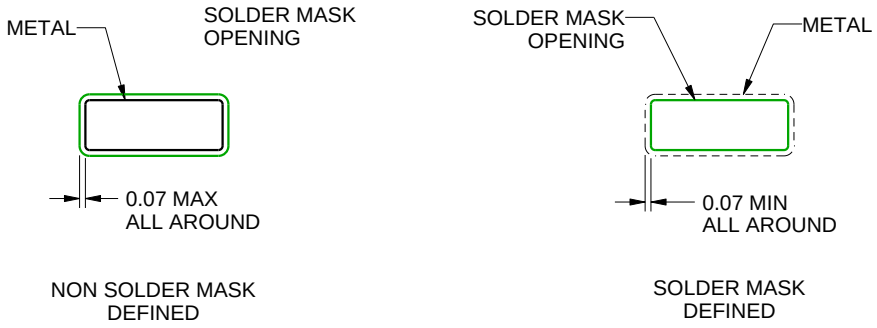


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X



SOLDER MASK DETAILS

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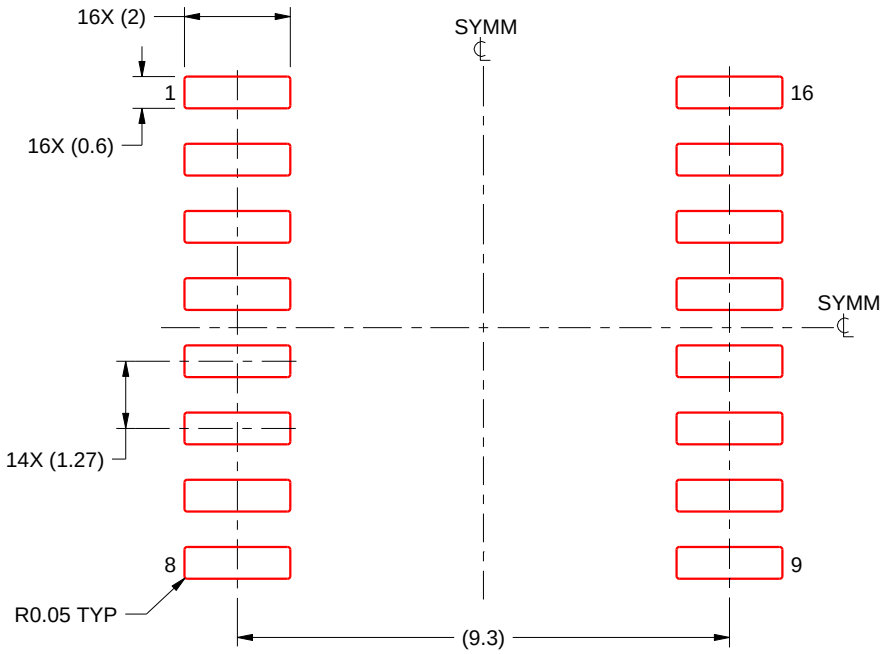
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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