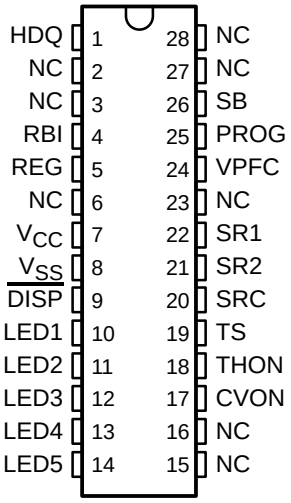
bq2016
GAS GAUGE IC FOR HIGH DISCHARGE RATES

SLUS475A – JANUARY 2001 – REVISED NOVEMBER 2002

- **Provides Accurate Measurement of Available Capacity in Nicd or NiMH Batteries**
- **Measures a Wide Dynamic-Current Range**
- **Requires ≤ 1 Square Inch of PCB Space for Easy Pack Integration**
- **Measures Charge Flow Using a Low-Offset V-to-F Converter**
- **Automatically Compensates Measurements for Rate and Temperature**
- **Supports 5 LEDs for Remaining Capacity Indication**
- **Provides a 1-Wire HDQ Communication Interface**
- **Packaging: 28-Pin SSOP**

TSSOP PACKAGE
(TOP VIEW)



NC — Do not connect

description

The bq2016 gas gauge IC for battery pack or in-system installation maintains an accurate record of available battery capacity. To integrate charge and discharge activity of the battery, the IC monitors a voltage drop across a sense resistor connected in series with the cells of the battery. The bq2016 compensates for battery temperature, charge/discharge rate, and battery self-discharge to the charge counter to provide available-capacity information across a wide range of operating conditions. The bq2016 works with NiCd or NiMH battery packs that have a capacity of 1 to 4.5 Ah and that are designed for high discharge rate applications such as power tools.

The VPFC input sets the initial full charge reference of the battery pack. The bq2016 learns the true discharge capacity of the battery pack and automatically updates the full-charge reference during the course of a discharge cycle from full to empty. The remaining capacity is reported as the ratio between the actual discharge capacity and the full-charge capacity. The bq2016 communicates available capacity using 5 LEDs or the 1-wire communications port.

The 1-wire serial communication port (5Kb/s) allows an external processor to read and write the internal registers of the bq2016. Communication with the bq2016 is useful for pack testing or host processing of the available battery information. The internal registers include available battery capacity, voltage, temperature, current, and battery status. The RBI input maintains the register set in the event of pack voltage collapse due to a high discharge pulse.

The bq2016 circuit can operate from the cells in the pack. The REG output and an external FET provide a simple, inexpensive voltage regulator to supply power to the circuit from the cells

OPTIONS

T_J	28-PIN SSOP PACKAGE
–20°C to 70°C	bq2016DBQ bq2016DBQR

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
HDQ	1	I/O	Serial communication input/output. Open-drain bidirectional communications port.
RBI	4	I	Register backup input provides backup potential to the bq2016 registers during periods of low operating voltage. RBI accepts a storage capacitor or a battery input.
REG	5	O	Regulator output provides a reference to control an n-JFET for VCC regulation to the bq2016 from the battery potential.
V_{CC}	7	I	Supply voltage input
V_{SS}	8		Ground
LED1–LED5	10–14	O	LED display segment outputs that each may drive an external LED.
CVON	17	O	Cell voltage divider control. Output to connect the voltage divider on the voltage input during measurement.
VPFC	24	I	Program capacity input. 16-level input to program the initial battery full-charge reference.
SB	26	I	Battery voltage input. Input connection to monitor battery–pack voltage.
SR2–SR1	21,22	I	Sense resistor inputs. Input connections for a small value sense resistor to monitor the battery charge and discharge current flow.
SRC	20	I	Current sense voltage input to monitor instantaneous current.
$\overline{DISP}$	9	I	Display activation input that activates the LED drivers LED1–LED5.
TS	19	I	Temperature sense input connects to an external thermistor or should be grounded when using the internal thermistor. The function depends on the state of the PROG input.
PROG	25	I	Program input defines the temperature measurement thermistor (internal or external).
THON	18	O	Thermistor bias control output to control a switch in series with an optional external thermistor.
NC	2, 3, 6, 15, 16, 23, 27, 28		Do not connect. For proper device operation, these pins should not be connected.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Relative to V_{SS}: V_{CC} ..... –0.3 V to 6 V
V_{IN} (All other pins) ..... –0.3 V to 6 V
Operating temperature, T_{OPR} ..... –20°C to 70°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

dc electrical characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage		2.7	3.3	3.7	V
I_{CC}	Operating current			180	235	μA
V_{OLS}	Sink voltage: LED1–LED5	I_{OLS} = 5 mA			0.4	V
V_{OLS}	Sink voltage: TI ION, CVON	I_{OLS} = 1 mA			0.36	V
V_{IL}	Input voltage low $\overline{DISP}$		–0.3		0.8	V
V_{IH}	Input voltage high $\overline{DISP}$		2.0		V_{CC} + 0.3	V
V_{OL}	Output voltage low HDQ	I_{OL} = 1 mA			0.4	V
V_{ILS}	Input voltage low HDQ		–0.3		0.8	V
V_{IHS}	Input voltage high HDQ		1.7		6.0	V
V_{AI}	Input voltage range SB, PROG, VPFC, TS		V_{SS}–0.3		V_{CC} + 0.3	V
I_{RB}	RBI data-retention input current	V_{RBI} > 3 V, V_{CC} < 2 V		10	50	nA
V_{RBI}	RBI data-retention voltage		1.3			V
Z_{AI1}	Input impedance: SR1, SR2	0–1.25V	10			MΩ
Z_{AI2}	Input impedance: SB, SRC	0–1.25V	5			MΩ
Z_{AI3}	Input impedance: PROG, VPFC	0–V_{CC}	5			MΩ

NOTE: Z_{AI} specifications are reference numbers based on process data.

VFC characteristics, V_{CC} = 3.1–3.5 V, T_{OPR} = 0°C to 70°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{SR}	Input voltage range, V_{SR2} and V_{SR1}	V_{SR} = V_{SR2} – V_{SR1}	–0.25		0.25	V
V_{SROS}	V_{SR} input offset	V_{SR2} = V_{SR1}, autocorrection disabled	–300	–50	300	μV
V_{SRCOS}	Calibrated offset	After autocorrection	–16		16	V
INL	Integral nonlinearity error	T_{OPR} = 0°C to 50°C			0.21%	

REG characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RO}	REG controlled output voltage	JFET: R_{ds}(on) < 150 Ω V_{gs} (off) < –3 V at 10 μA	3.1	3.3	3.5	V
I_{REG}	REG output current		1			μA

serial communication timing parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(CYCH)}$	Cycle time, host to bq2016 (write)		190			µs
$t_{(CYCB)}$	Cycle time, bq2016 to host (read)		190	205	250	µs
$t_{(STRH)}$	Start hold, host to bq2016 (write)		5			ns
$t_{(STRB)}$	Start hold, bq2016 to host (read)		32			µs
$t_{(DSU)}$	Data setup time				50	µs
$t_{(DSUB)}$	Data setup time				50	µs
$t_{(DH)}$	Data hold time		90			µs
$t_{(DV)}$	Data valid time		80			µs
$t_{(SSU)}$	Stop setup time				145	µs
$t_{(SSUB)}$	Stop setup time				145	µs
$t_{(RSPS)}$	Response time, bq2016 to host		320			µs
$t_{(B)}$	Break		190			µs
$t_{(BR)}$	Break recovery		40			µs

timing requirements

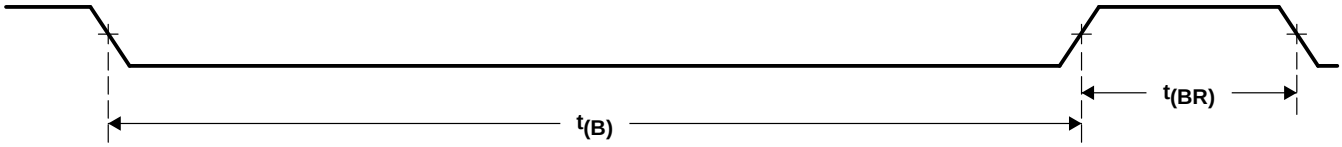


Figure 1. Break Timing

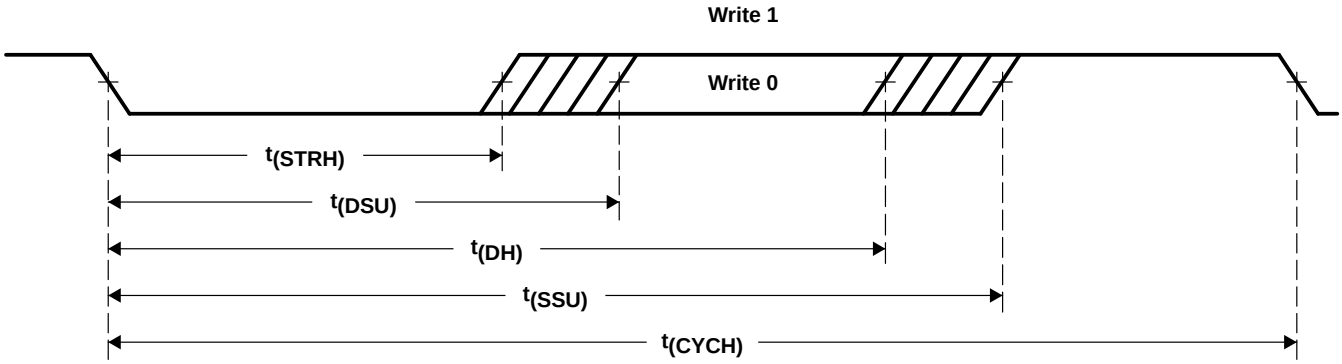


Figure 2. Host to bq2016

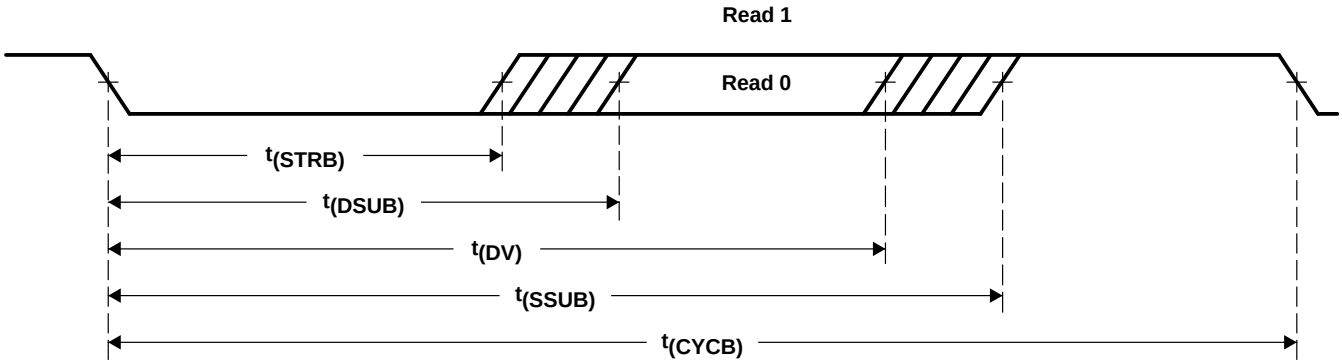


Figure 3. bq2016 to Host

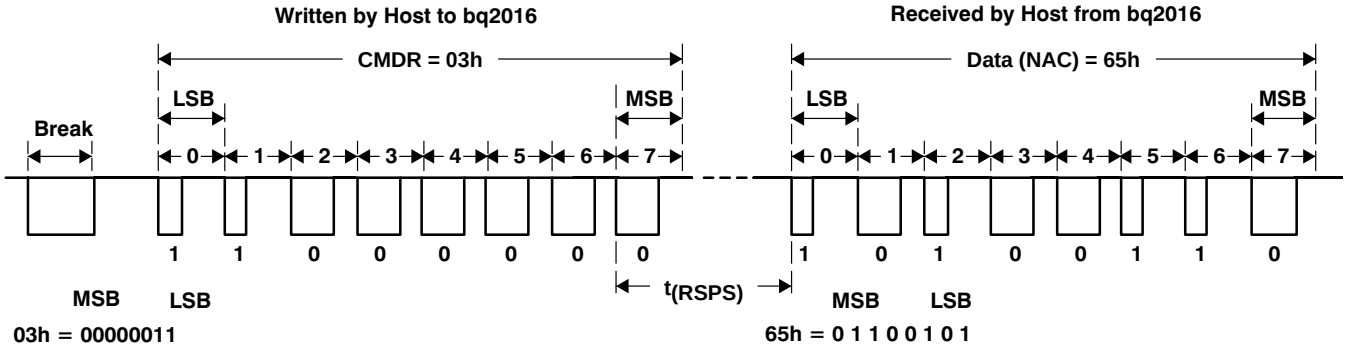


Figure 4. Typical Communication With the bq2016

functional description

general operation

The bq2016 determines battery capacity by monitoring the amount of charge input to or removed from a rechargeable battery. The bq2016 measures charge and discharge currents, estimates self-discharge, and monitors the battery for low voltage and capacity thresholds. The bq2016 automatically compensates charge and discharge currents for rate and temperature to adjust for battery efficiency under different conditions.

The bq2016 is configured to display capacity in a relative display mode. The display mode uses the last measured discharge or learned capacity of the battery as the battery-full reference. The LED display can be activated by a push-button connected to the $\overline{\text{DISP}}$ input or when the bq2016 detects a charge or discharge rate.

measurements

The bq2016 uses a fully differential, dynamically balanced voltage-to-frequency converter (VFC) for charge measurement and a delta sigma analog-to-digital converter (ADC) for battery voltage, current, and temperature measurement.

charge and discharge counting

The VFC measures the charge and discharge flow of the battery by monitoring a small-value sense resistor between the SR1 and SR2. The VFC measures bipolar signals up to 250 mV in magnitude. The bq2016 detects charge activity when $V_{SR} = V_{SR2} - V_{SR1}$ is positive and a discharge activity when $V_{SR} = V_{SR2} - V_{SR1}$ is negative. The bq2016 integrates the signal over time using an internal counter. The bq2016 accumulates charge or discharge at the rate of 3.125 μVh.

digital filter and VFC calibration

The bq2016 does not integrate charge or discharge counts below the digital filter threshold. The digital filter threshold is set at 300 μV until a VFC calibration is performed. The calibration is performed after the first valid charge after initialization. It takes up to 20 minutes to begin the calibration and up to 60 minutes to complete the VFC calibration. The bq2016 suspends VFC calibration while it detects charge or discharge activity during this period. After successful VFC calibration, the digital filter threshold is set to 100 μV.

voltage monitoring and thresholds

In conjunction with monitoring SR1 and SR2 for charge and discharge currents, the bq2016 monitors the battery pack potential through the SB pin. The bq2016 measures the pack voltage and reports the result in the battery voltage (VSBH:L) register. The bq2016 converts the signals at the SB input every 2 seconds.

The SB input is divided down from the cells using 1% tolerance resistors. To reduce current consumption from the battery, the CVON output can switch the divider to the cells only during measurement period. CVON is high impedance when the cells are measured, and driven low otherwise. The full-scale input for the SB pin is 1.25 V.

The bq2016 monitors the voltage at SB for the end-of-discharge voltage (EDV) and maximum voltage (MCV) thresholds. The bq2016 uses the EDV threshold level to determine when the battery has reached an empty state, and the MCV threshold level to detect a fault condition during charge. The EDV and MCV input levels are set at:

EDV = 0.45 V
MCV = 1.00 V

The bq2016 disables EDV monitoring if V_{SR} is greater than the overload threshold. If the bq2016 detects an overload threshold, the bq2016 sets the OLVD flag in the secondary status flags (FLAGS2) register. The bq2016 resumes EDV detection after V_{SR} drops back below the overload threshold. The overload threshold is a function of battery capacity and is defined in the PFC table.

functional description (continued)

current

The SRC input of the bq2016 measures battery charge and discharge current. The SRC ADC input converts the current signal from the series sense resistor every 2 seconds and stores the result in the current scale register (VSRH:L). The full scale input range to SRC is limited to ±250 mV as shown in Table 1.

Table 1. SRC Input Range

SENSE RESISTOR (mΩ)	FULL SCALE INPUT (±A)
5	50
7.5	33
10	25

temperature

The bq2016 measures temperature, either with its internal thermistor or with an external thermistor, depending on the state of the PROG input. The bq2016 accepts an external NTC thermistor on the TS input. The bq2016 samples the TS input voltage every 2 seconds and stores the voltage in the TS Input Voltage (TEMPVH:L) register and the actual temperature in the temperature (TEMP) register. With an external thermistor, the bq2016 develops the temperature value for the temperature register on the basis of a Semitec 103AT (10K) NTC model. The bq2016 reports the temperature in 1°C steps with an accuracy of 4°C or 6°C for an external and internal thermistor, respectively. The temperature reading is used to adapt remaining capacity for charge and discharge efficiency and to adjust for the battery's self discharge.

If an internal thermistor is selected for temperature measurement, the TS input should be grounded.

THON may be used to connect the bias source to the thermistor when the bq2016 samples the TS input. THON is high impedance when the temperature is measured, and driven low otherwise.

gas gauge operation

general

The operational overview diagram in Figure 5 illustrates the operation of the bq2016. The bq2016 accumulates a measure of charge and discharge currents and estimates self-discharge. The bq2016 compensates the charge and discharge currents for rate and temperature efficiencies. It also adjusts the self-discharge estimation for temperature variation. The bq2016 stores the compensated charge accumulation in the nominal available capacity (NAC) register. For LED indication, the bq2016 adjusts NAC for the battery pack operating temperature.

The discharge count register (DCR) tracks discharge activity of the battery. The last measured discharge (LMD) represents the discharge capacity or learned full capacity of the battery in the application. The bq2016 transfers the value in DCR to LMD when a qualified discharge occurs.

functional description (continued)

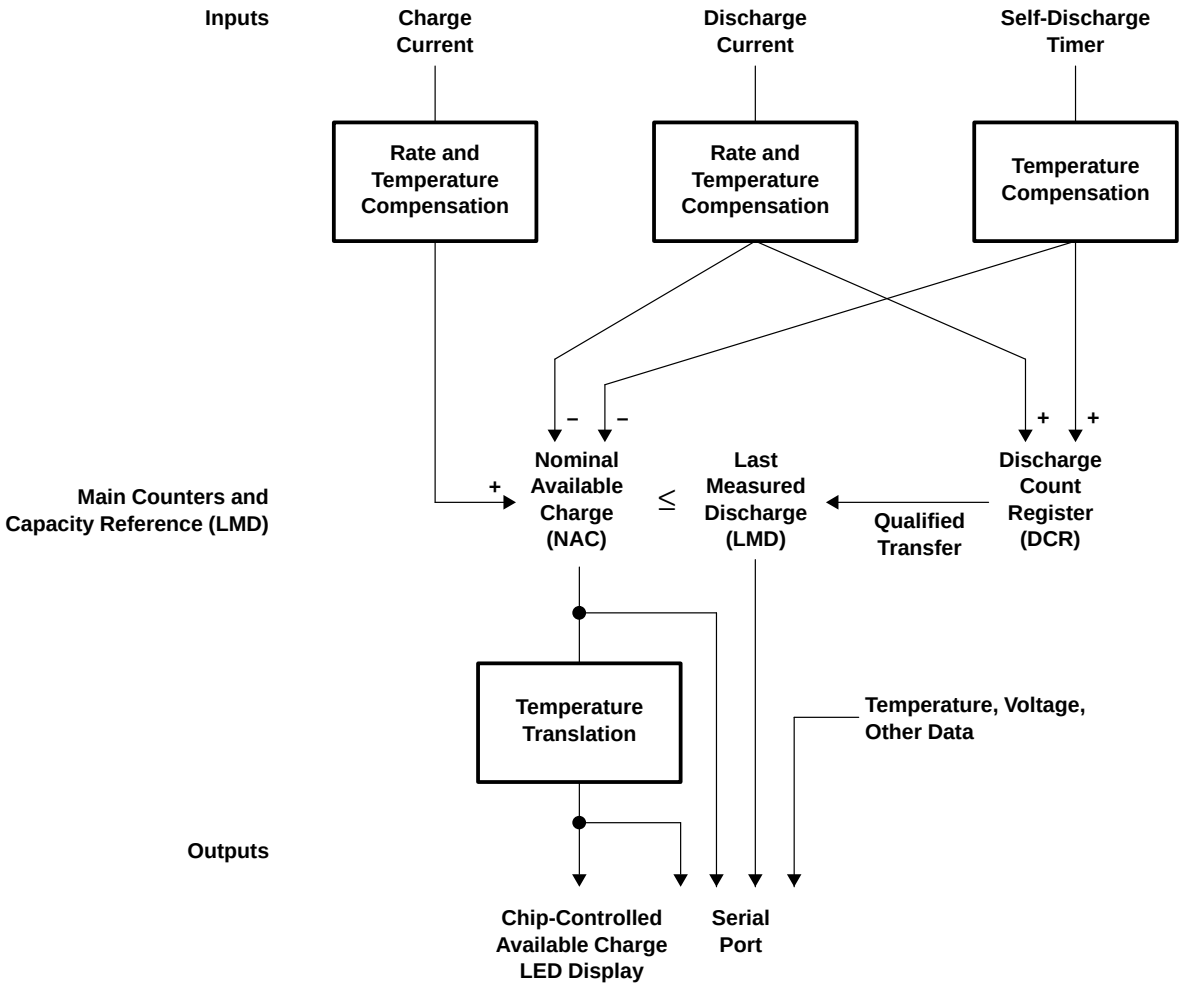


Figure 5. Operational Overview Diagram

main gas gauge registers

programmed full count (PFC)

The programmed full count (PFC) register stores the user-specified battery full capacity. The 8-bit PFC registers stores the full capacity in mVh scaled as shown in Table 2. The VPFC input sets the PFC value and the counting scale on a bq2016 initialization (power on reset).

nominal available capacity (NAC)

The main counter, NAC, represents the available battery capacity at any given time. Battery charging increments the NAC register, while battery discharging and self-discharge decrement the NAC register. The bq2016 compensates the charge and discharge inputs to NAC for rate and temperature efficiencies.

NAC counts up during charge to a maximum value of LMD and down during discharge and self-discharge to 0. The bq2016 resets NAC to 0 on initialization and when the bq2016 sets the EDV bit on discharge. To prevent overstatement of charge during periods of overcharge, NAC stops incrementing when NAC = LMD.

main gas gauge registers (continued)

NAC calibration

The bq2016 sets NAC to 85% of LMD when it detects a transition from fast-charge to a trickle charge provided that 85% ≥ NAC > 80% of LMD when the bq2016 detects the transition. For this determination, fast-charge detection (FCDT) corresponds to the FCDT value set by the PROG pin. Fast-charge detection occurs when the FCDT condition is met for 30s after the CHGS bit is set in FLGS1. Once fast-charge activity is qualified, a transition of the SRC signal below the FCDT threshold enables trickle-charge detection. The bq2016 verifies trickle charge by continuing to sample the SRC input for signals above the trickle-charge threshold and below the fast-charge threshold. This sampling can take up to 3 minutes. Once a trickle-charge is verified, the bq2016 adjusts NAC up to 85% of LMD if NAC was between 80% and 85% of LMD. If NAC was greater then 85% of LMD, NAC is unchanged upon transition detection.

last measured discharge (LMD)

Last measured discharge is the most recent measured discharge capacity of the battery. On initialization, the bq2016 sets LMD = PFC. When a valid charge is detected following a valid discharge, the bq2016 updates LMD with the current value in DCR. During subsequent discharges, the bq2016 updates LMD with the current value in DCR. (The DCR value represents the measured discharge capacity of the battery from full to the EDV threshold.) The bq2016 limits the adjustment of LMD down to 75% of its previous value. A qualified discharge is necessary for a capacity transfer from DCR to the LMD register. The LMD register also serves as the 100% reference threshold used by the display mode.

discharge count register (DCR)

The discharge count register (DCR) is used to update the last measured discharge register only if a complete battery discharge from full to empty occurs without any partial battery charges. In this way, the bq2016 adapts its capacity determination based on the actual conditions of discharge.

The DCR counts up during discharge independent of NAC and can continue to increase after NAC decrements to 0. Before NAC = 0 (empty battery), both discharge and self-discharge increment the DCR. After NAC = 0, only discharge increments the DCR. The DCR resets to 0 when the VDQ bit in the primary status flags register (FLAGS1) is set on charge. The bq2016 sets VDQ=1 on a fast charge-to-trickle detection if NAC is greater than 80% of LMD or when NAC=LMD. The DCR does not roll over but stops counting when it reaches ffffh. The DCR value becomes the new LMD value on the first valid charge after a discharge to EDV threshold if the bq2016 detects a qualified discharge. A valid charge is a minimum of one (maximum of two) NAC increments. A qualified discharge occurs if

- No valid charge initiations occurred during the period between when VDQ gets set on charge and when the bq2016 detects EDV on discharge.
- The self-discharge count is not more than 10% of PFC.
- The temperature is greater than or equal to 0°C when the EDV level is reached during discharge.
- The EDV bit gets set.

The VDQ bit set to a one indicates whether the present discharge is valid for LMD update.

programming the bq2016

The bq2016 is programmed with the VPFC and the PROG pins. During power-up or initialization, the bq2016 reads the state of these multilevel inputs and latches in the programmable configuration settings. Resistor divider networks for VPFC and PROG should target the nominal thresholds as defined in the programming tables.

programmable configuration settings

design capacity

The battery's rated design capacity or programmed full count (PFC) is programmed with the VPFC pin as shown in Table 2, and represents the battery's full reference. The VPFC pin is a 16-level input.

Table 2. PFC Selections

PFC LEVEL	LOWER	NOMINAL THRESHOLD (V_{CC})	UPPER	PFC (COUNT)	SCALE (mVh/ COUNT)	CAPACITY (mVh)	OVERLOAD THRESHOLD (mV)	Rv (kΩ)	Rg (kΩ)	CHEMISTRY
1	0/32	≤ 1/32 <	2/32	30720	1/2560	12.0	50	Open	0	NiCd
2	2/32	≤ 3/32 <	4/32	25344	1/2560	9.9	50	1000	102	NiCd
3	4/32	≤ 5/32 <	6/32	41472	1/5120	8.1	50	1000	187	NiCd
4	6/32	≤ 7/32 <	8/32	33792	1/5120	6.6	50	1000	280	NiCd
5	8/32	≤ 9/32 <	10/32	27648	1/5120	5.4	30	1000	392	NiCd
6	10/32	≤ 11/32 <	12/32	46080	1/10240	4.5	30	1000	523	NiCd
7	12/32	≤ 13/32 <	14/32	36864	1/10240	3.6	30	1000	681	NiCd
8	14/32	≤ 15/32 <	16/32	30720	1/10240	3.0	30	1000	887	NiCd
9	16/32	≤ 17/32 <	18/32	39936	1/10240	3.9	30	887	1000	NiMH
10	18/32	≤ 19/32 <	20/32	46080	1/10240	4.5	30	681	1000	NiMH
11	20/32	≤ 21/32 <	22/32	27648	1/5120	5.4	30	523	1000	NiMH
12	22/32	≤ 23/32 <	24/32	33792	1/5120	6.6	30	392	1000	NiMH
13	24/32	≤ 25/32 <	26/32	39936	1/5120	7.8	50	280	1000	NiMH
14	26/32	≤ 27/32 <	28/32	47616	1/5120	9.3	50	187	1000	NiMH
15	28/32	≤ 29/32 <	30/32	28416	1/2560	11.1	50	102	1000	NiMH
16	30/32	≤ 31/32 ≤	32/32	33792	1/2560	13.2	50	0	Open	NiMH

The correct PFC may be determined by multiplying the rated battery capacity in mAh by the sense-resistor value:

Battery capacity (mAh) × sense resistor (Ω) = PFC (mVh)

Selecting a PFC slightly less than the rated capacity provides a conservative capacity reference. The bq2016 stores the selected PFC in the PFC register.

programmable configuration settings (continued)

internal or external thermistor

The PROG pin programs whether the bq2016 uses an internal or external thermistor according to the following table. It also defines the fast charge and trickle-rate detection thresholds for NAC calibration.

Table 3. PROG Selections

PROG LEVEL	LOW	NOM (V_{CC})	HI	T	TRICKLE RATE	FAST CHARGE DETECTION THRESHOLD (FCDT)	Rv (k)	Rg (k)
1	0/12	≤ 1/12 <	2/12	I	VDMF < V_{SR} < 2 mV	V_{SR} > 2 mV for 30s	Open	0
2	2/12	≤ 3/12 <	4/12	I	VDMF < CRate < C/8	CRate > C/5 for 30s	1000	332
3	4/12	≤ 5/12 <	6/12	I	—	—	1000	715
4	6/12	≤ 7/12 <	8/12	E	VDMF < V_{SR} < 2 mV	> 2 mV for 30s	715	1000
5	8/12	≤ 9/12 <	10/12	E	VDMF < CRate < C/8	CRate > C/5 for 30s	332	1000
6	10/12	≤ 11/12 ≤	12/12	E	—	—	0	Open

NOTE: The bq2016 does not perform NAC calibration on charge with options 3 and 6. VDMF = 300 μV uncalibrated or 100 μV calibrated.

programming example

Given:

Sense resistor = 0.003 Ω
Chemistry = NiCd
Capacity = 2000 mAh
Discharge current range = 1 A to 10 A
Charge current = 200 mA to 4 A
Voltage drop over sense resistor = –30 mV to 12 mV
Internal thermistor with 2 mV FCDT

Therefore

2000 mAh × 0.003 = 6 mVh

Select

VPFC level = 5
PROG level = 1
TS pin = grounded

The initial full battery capacity is 5.4 mVh (1800 mAh) until the bq2016 *learns* a new capacity with a qualified discharge from full to EDV.

charge and discharge count counting

charge counting

The bq2016 detects charge activity when $V_{SR} = V_{SR2} – V_{SR1}$ is greater than the digital filter threshold. If charge activity is detected, the bq2016 increments NAC at a rate proportional to VSR and activates the LED display if $V_{SR} > 2$ mV. Charge actions increment the NAC after compensation for charge rate and temperature. Charge counting continues until V_{SR} drops below VDMF.

discharge counting

The bq2016 detects discharge activity when $V_{SR} = V_{SR2} – V_{SR1}$ is more negative than the digital filter threshold. If discharge activity is detected, the bq2016 decrements NAC and increments DCR at a rate proportional to V_{SR} and activates the LED display if $V_{SR} < –2$ mV. Discharge actions decrement NAC and increment DCR after compensation for discharge rate and temperature. Discharge counting continues until V_{SR} rises above –VDMF.

charge and discharge count counting (continued)

self-discharge estimation

The bq2016 continuously decrements NAC and increments DCR for self-discharge based on time and temperature. The self-discharge count rate is programmed to be a nominal 1/80 × NAC rate per day for NiCd and a nominal 1/60 × NAC for NiMH. This is the rate for a battery whose temperature is between 20°C–30°C. The self-discharge rate doubles every 10°C increase in temperature.

count compensations

The bq2016 compensates charge and discharge counting for temperature and rate before updating the NAC and/or DCR. The bq2016 compensates self-discharge estimation for temperature before updating the NAC or DCR.

charge compensations

The bq2016 compensates for charge efficiencies at a quick-charge and fast-charge rate at two different temperature thresholds. The bq2016 applies the NiCd or NiMH factors based on the VPFC setting. For charge compensation, quick charge is defined as a C/5 charge rate or less and fast charge is defined as a rate greater than C/5.

The charge-compensation factors are shown in Tables 4 and 5.

charge compensations

Table 4. Charge Compensation for NiCd

CHARGE TEMPERATURE	QUICK CHARGE (≤ C / 5) COMPENSATION	FAST CHARGE (> C / 5) COMPENSATION
<40C	0.80	0.95
≥ 40	0.75	0.90

Table 5. Charge Compensation for NiMH

CHARGE TEMPERATURE	QUICK CHARGE (≤ C / 5) COMPENSATION	FAST CHARGE (> C / 5) COMPENSATION
<40C	0.80	0.90
≥ 40	0.75	0.85

discharge compensation

The bq2016 corrects for the rate of discharge by adjusting an internal discharge-compensation factor. The discharge factor is based on the calculated discharge rate determined from the V_{SR} potential and the PFC setting. The table below shows the compensation factors for NiCd and NiMH during discharge:

DISCHARGE RATE	DISCHARGE EFFICIENCY (F_{DE}) (%)
≤1C	100
>3C	100
>6C	95
>9C	95
>12C	90

NOTE: The C Rate determination is made from LMD.

discharge compensation (continued)

The bq2016 adjusts the discharge-compensation efficiency for temperature. At lower temperatures, the discharge-efficiency factor decreases by 5% for each 10°C temperature step below 10°C.

$$F_{DE\ (new)} = F_{DE} - (5\% \times N)$$

where N = number of 10°C steps below 10°C.

For example at a 1C discharge,

T > 10°C:	N = 0 and $F_{DE(NEW)}$ = 100%
0°C < T < 10°C:	N = 1 and $F_{DE(NEW)}$ = 95%
–10°C < T < 0°C:	N = 2 and $F_{DE(NEW)}$ = 90%
–20°C < T < –10°C:	N = 3 and $F_{DE(NEW)}$ = 85%
–20°C < T < –30°C:	N = 4 and $F_{DE(NEW)}$ = 80%

error summary

capacity inaccurate

The LMD is susceptible to error on initialization or if no updates occur. On initialization, the LMD value includes the error between the programmed full capacity and the actual capacity. This error is present until a valid discharge occurs and LMD is updated. The other cause of LMD error is battery wear-out. As the battery ages, the measured capacity must be adjusted to account for changes in actual battery capacity. The bq2016 increments the capacity inaccurate count (CPI) register each time a valid charge occurs and is reset whenever LMD is updated from the DCR. The counter does not wrap around but stops counting at 255. The capacity inaccurate flag (CI) is set if LMD has not been updated following 64 valid charges.

display

The bq2016 can directly display capacity information using low-power LEDs. The bq2016 displays the battery charge as a percentage of the LMD.

The capacity display is also adjusted for the present battery temperature. The temperature adjustment reflects the available capacity at a given temperature but does not affect the NAC register. Tables 6 and 7 show the temperature adjustments:

Table 6. Temperature Translation for NiCd

TEMPERATURE (C)	TEMPERATURE TRANSLATION (%)
T ≥ 10	100
10 > T ≥ 0	100
0 > T ≥ –10	90
–10 > T ≥ –20	75
T < –20	50

Table 7. Temperature Translation for NiMH

TEMPERATURE (C)	TEMPERATURE TRANSLATION (%)
T ≥ 10	100
10 > T ≥ 0	75
0 > T ≥ –10	40
–10 > T ≥ –20	0
T < –20	0

error summary (continued)

The display becomes active during charge if the NAC registers are counting at a rate equivalent to $V_{SR} > 2$ mV or discharge if the NAC registers are counting at a rate equivalent to $V_{SR} < –2$ mV. When $\overline{DISP}$ is pulled low, the segment output becomes active for 4 seconds. LED1 blinks at a 4-Hz rate whenever NAC is less than 6% of LMD or $V_{SB} \leq V_{EDV}$.

Table 8. Display Mode

LED1	LED2	LED3	LED4	LED5	NAC / LMD
ON	ON	ON	ON	ON	80 – 100%
ON	ON	ON	ON	OFF	60 – < 80%
ON	ON	ON	OFF	OFF	40 – < 60%
ON	ON	OFF	OFF	OFF	20 – < 40%
ON	OFF	OFF	OFF	OFF	6 < 20%
BLINK	OFF	OFF	OFF	OFF	< 6%
BLINK	OFF	OFF	OFF	OFF	$V_{SB} \leq V_{EDV}$

RBI input

The RBI input pin should be used with a storage capacitor or external supply to provide backup potential to the internal bq2016 registers when V_{CC} drops below 3.0 V. V_{CC} is output on RBI when V_{CC} is above 3.0 V. If an external supply (such as the bottom series cell) is the backup source, then an external diode is required for isolation.

initialization

The bq2016 can be initialized by removing VCC and grounding the RBI pin for 5 seconds or by a command over the serial port. The HDQ port reset command requires writing 78h to register CMDWD.

microregulator

A REG output is provided to regulate an external low-threshold JFET to supply power to the bq2016 based circuit from the series cells. The REG output maintains VCC to the bq2016 at 3.3 V.

communicating with the bq2016

The bq2016 includes a simple single-pin (HDQ referenced to Vss) serial data interface. A host processor uses the interface to access various bq2016 registers. By adding a single contact to the battery pack, the host can easily monitor the battery characteristics. The open-drain HDQ pin on the bq2016 should be pulled up by the host system or pulled down to ground.

The interface uses a command-based protocol, in which the host processor sends a command byte to the bq2016. The command directs the bq2016 to either store the next eight bits of data received to a register specified by the command byte or output the eight bits of data specified by the command byte. The communication protocol is asynchronous return-to-one. Command and data bytes consist of a stream of eight bits that have a maximum transmission rate of 5K bits/s. The least-significant bit of a command or data byte is transmitted first. The protocol is simple enough that it can be implemented by most host processors using either polled or interrupt processing. Data input from the bq2016 may be sampled using the pulse-width capture timers available on some microcontrollers.

If a communication error occurs (e.g., $t_{CYCB} > 250\mu s$), the bq2016 should be sent a BREAK to reinitiate the serial interface. A BREAK is detected when the HDQ pin is driven to a logic-low state for a time t_B or greater. The HDQ pin should then be returned to its normal ready-high logic state for a time t_{BR}. The bq2016 is now ready to receive a command from the host processor.

communicating with the bq2016 (continued)

The return-to-one data bit frame consists of three distinct sections. The first section is used to start the transmission by either the host or the bq2016 taking the HDQ pin to a logic-low state for a period $t_{STRH;B}$. The next section is the actual data transmission, where the data should be valid by a period $t_{DSU;B}$, after the negative edge used to start communication. The data should be held for a period $t_{DH;DV}$, to allow the host or bq2016 to sample the data bit.

The final section is used to stop the transmission by returning the HDQ pin to a logic-high state by at least a period $t_{SSU;B}$, after the negative edge used to start communication. The final logic-high state should continue during a period $t_{CYCH;B}$, to allow time to ensure that the bit transmission was stopped properly. The timings for data and break communication are given in the serial communication timing specification and illustration sections.

In communication with the bq2016 the least-significant bit is always transmitted first.

command code and registers

The bq2016 status registers are listed in Table 9 and are described below.

command code

The bq2016 latches the command code when eight valid command bits have been received by the bq2016. The command code contains two fields:

- W/$\overline{R}$ bit
- Command address

The W/$\overline{R}$ bit of the command code determines whether the received command is for a read or a write function.

command code (continued)

W/$\overline{R}$ is:

0 The bq2016 outputs the requested register contents specified by the address portion of command code.
1 The host writes to the register specified by the address portion of the command code.

The lower seven-bit field of the command code contains the address portion of the register to be accessed. The bq2016 ignores writes to invalid addresses.

registers

FLAGS1 (0x01) – Primary Status Flags

The FLAGS1 register provides bq2016 status information. The 8-bit register includes the following status bits:

7	6	5	4	3	2	1	0
CHGS	BRP	MCV	CI	VDQ	RSVD	EDV	OCE

CHGS

The bq2016 set the CHGS bit when it detects charge activity. The bq2016 clears the CHGS bit on discharge.

Bit = Condition
0 The bq2016 detects discharge.
1 The bq2016 detects charge.

BRP

The bq2016 sets the BRP bit when it performs a full reset.

registers (continued)

MCV
The bq2016 sets the MCV bit when it detects that the maximum cell voltage threshold is being exceeded.

Bit =	Condition
0	Cell voltage is below the threshold.
1	Cell voltage is above the threshold.

CI
The bq2016 sets the CI bit on reset and when the CPI register exceeds 64.

Bit =	Condition
0	An LMD update has occurred.
1	The bq2016 has been reset or the CPI register exceeds 64.

VDQ
The bq2016 sets the VDQ bit when the present discharge cycle is considered valid for an LMD update.

Bit =	Condition
0	The present discharge cycle is not valid for an LMD update.
1	The present discharge cycle is valid for an LMD update.

Bit 2 is reserved.

EDV
The bq2016 sets the EDV bit when the battery voltage drops below the EDV threshold. The bit is latched and remains set until valid charge activity is detected.

Bit =	Condition
0	The battery voltage is greater than the EDV threshold.
1	The battery voltage is less than the EDV threshold.

OCE
The bq2016 sets the OCE bit when an VFC offset calibration has been performed.

Bit =	Condition
0	Offset calibration not completed
1	Offset calibration completed

TEMP (0x02) – Temperature
The TEMP register contains the battery temperature as computed using the internal temperature sensor of the bq2016. It is represented in degrees C. The data is an 8-bit signed integer. For example, –10°C is represented as F6h.

NAC (0x03) – Nominal Available Capacity
NAC is an 8-bit register that contains the present remaining capacity of the battery pack. The NAC contents are compensated for rate and temperature. The data is represented in the same units as PFC.

LMD (0x05) – Last Measured Discharge
LMD stores the *learned* discharge capacity of the battery pack and represents the full charge reference. The 8-bit register presents data in the same units as PFC.

FLAGS2 (0x06) – Second Status Flags
The FLAGS2 register provides bq2016 status information. The 8-bit register includes the following status bits:

7	6	5	4	3	2	1	0
RSVD	DR2	DR1	DR0	RSVD	RSVD	RSVD	OVLD

registers (continued)

DR2–0

The DR2–0 bits represent the present discharge rate of the battery according to the following code:

DISCHARGE RATE INDICATION			
DISCHARGE RATE (R)	**DR2**	**DR1**	**DR0**
R ≤ 1C	0	0	0
1C < R ≤ 3C	0	0	1
3C < R ≤ 6C	0	1	0
6C < R ≤ 9C	0	1	1
9C < R ≤ 12C	1	0	0
R > 12C	1	0	1

OVLD

The bq2016 set the OVLD bit when it detects that the present discharge rate exceeds the programmed overload threshold.

Bit = Condition
0 Discharge rate is below the overload threshold.
1 Discharge rate is above the overload threshold.

VPFC (0x07) – VPFC Pin Input Level

VPFC stores the input level at the VPFC programming pin. The voltage at the VPFC (V_{VPFC}) pin is calculated by

$$V_{VPFC}\ (mV) = Vcc \times (V_{PFC}/256)$$

VPROG (0x08) – VPROG Pin Input Level

VPROG stores the input level at the VPROG programming pin. The voltage at the VPROG (V_{PROG}) pin is calculated by:

$$V_{VPROG}\ (mV) = Vcc \times (V_{PROG}/256)$$

CPI (0x09) – Capacity Input Level

CPI stores the number of valid charge actions since the last LMD update.

OCTL (0x0a) – Output Control

OCTL provides a means of testing LED functionality. The register consists of:

7	6	5	4	3	2	1	0
RSVD	RSVD	OCTL5	OCTL4	OCTL3	OCTL2	OCTL1	$\overline{\text{Enable}}$

When $\overline{\text{Enable}}$ is low, the bq2016 writes the data in OCTL5–1 to the LED5–1 pins. A one in OCTL5–1 turns the corresponding LED on. This function overrides the LED indication as a representation of capacity.

FULCNT (0x0b) – Full Count Register

FULCNT store the number of times the battery has been charged to full (NAC=LMD) in 16 count increments.

CMDWD (0x0c) – Command Word

The CMDWD register can be used to reset the bq2016 or initiate a VFC offset calibration.

To reset the bq2016, 0x78 must be written to this location. When reset, the bq2016 sets the following values:

NAC = 0
LMD = PFC
CPI = 0
FULCNT = 0
DCR = 0

To calibrate the VFC, 0x68 must be written to this location. During VFC offset calibration, the bq2016 deselects the SR1 and SR2 inputs and disables the LEDs. When the bq2016 successfully completes VFC calibration, it sets the OCE bit in FLAGS1. The command 0x60 terminates a VFC calibration. The bq2016 automatically performs VFC calibration after trickle detection and initial power-up, and when NAC = LMD.

PFC (0x0f) – Programmed Full Count
The PFC register stores the battery design capacity as defined by the VPFC input.

VSB (0x10 and 0x11) – Battery Voltage
VSBH (0x11) and VSBL (0x10) form the 16-bit register that contains the voltage present at the SB input pin in mV.

VSR (0x12 and 0x13) – Current Scale
VSRH (0x13) and VSBL (0x12) form the 16-bit register that contains the voltage present across the SR inputs pin in mV.

TEMPV (0x14 and 0x15) – Thermistor Voltage
TEMPVH (0x15) and TEMPVL (0x14) form the 16-bit register that contains the voltage present at the TS inputs pin in mV.

DCR (0x18) – Discharge Count Register
DCR stores the cumulative discharge count from the time VDQ is set on a charge. The data is represented in the same units as PFC. The number of counts equals DRC $\times$ 256.

FLAGS3 (0x4c) – Third Status Flags
The FLAGS3 register provides bq2016 status information. The 8-bit register includes the following status bits:

7	6	5	4	3	2	1	0
RSVD	RSVD	RSVD	RSVD	VQ	CR1	CR0	RSVD

CR1–CR0
The CR1–CR0 bits represent the present charge rate of the battery according to the following code:

CHARGE RATE INDICATION		
CHARGE RATE (R)	**CR1**	**CR0**
R ≤ C / 8	0	0
C / 5 ≥ R > C / 8	0	1
R > C / 5	1	1

VQ
The bq2016 sets the VQ bit when it detects a valid charge condition. A valid charge is two NAC increments.

Bit = Condition
0 = No valid charge condition
1 = Valid charge condition present

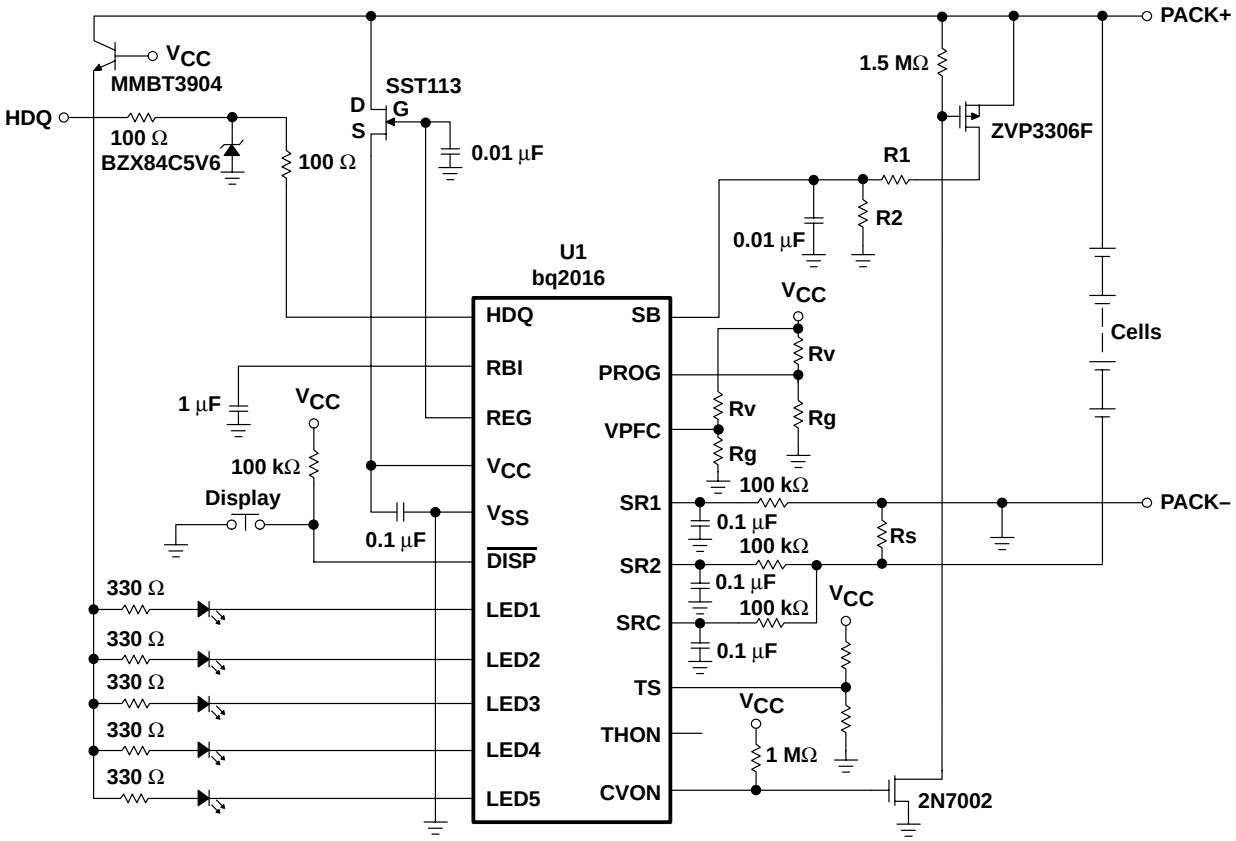
registers (continued)

Table 9. Command and Status Registers

SYMBOL	REGISTER NAME	LOC (HEX)	READ/ WRITE	7	6	5	4	3	2	1	0
FLAGS1	Primary status flags	0x01	R	CHGS	BRP	MCV	CI	VDQ	RSVD	EDV	OCE
TEMP	Temperature	0x02	R	TP7	TP6	TP5	TP4	TP3	TP2	TP1	TP0
NAC	Nominal available charge	0x03	R/W	NCH7	NCH6	NCH5	NCH4	NCH3	NCH2	NCH1	NCH0
LMD	Last measured discharge	0x05	R/W	LMD7	LMD6	LMD5	LMD4	LMD3	LMD2	LMD1	LMD0
FLAGS2	Secondary status flags	0x06	R	RSVD	DR2	DR1	DR0	RSVD	RSVD	RSVD	OVLD
VPFC	VPFC pin input level	0x07	R	VPFC7	VPFC6	VPFC5	VPFC4	VPFC3	VPFC2	VPFC1	VPFC0
VPROG	PROG pin input level	0x08	R	VPRO7	VPRO6	VPRO5	VPRO4	VPRO3	VPRO2	VPRO1	VPRO0
CPI	Capacity inaccurate count	0x09	R	CPI7	CPI6	CPI5	CPI4	CPI3	CPI2	CPI1	CPI0
OCTL	LED output control	0x0a	R/W	NA	NA	OCTL5	OCTL4	OCTL3	OCTL2	OCTL1	$\overline{\text{Enable}}$
FCNT	Full count register	0x0b	R/W	FCNT7	FCNT6	FCNT5	FCNT4	FCNT3	FCNT2	FCNT1	FCNT0
CMDWD	Command word	0x0c	R/W	CMD7	CMD6	CMD5	CMD4	CMD3	CMD2	CMD1	CMD0
PFC	Program PFC	0x0f	R/W	PFC7	PFC6	PCF5	PFC4	PFC3	PFC2	PFC1	PFC0
VSBL	Battery voltage (low byte)	0x10	R	VSBL7	VSBL6	VSBL5	VSBL4	VSBL3	VSBL2	VSBL1	VSBL0
VSBH	Battery voltage (high byte)	0x11	R	VSBH7	VSBH6	VSBH5	VSBH4	VSBH3	VSBH2	VSBH1	VSBH0
VSRL	Current scale (low byte)	0x12	R	VSRL7	VSRL6	VSRL5	VSRL4	VSRL3	VSRL2	VSRL1	VSRL0
VSRH	Current scale (high byte)	0x13	R	VSRH7	VSRH6	VSRH5	VSRH4	VSRH3	VSRH2	VSRH1	VSRH0
TEMPVL	TS input voltage (low byte)	0x14	R	TPVL7	TPVL6	TPVL5	TPVL4	TPVL3	TPVL2	TPVL1	TPVL0
TEMPVH	TS input voltage (high byte)	0x15	R	TPVH7	TPVH6	TPVH5	TPVH4	TPVH3	TPVH2	TPVH1	TPVH0
DCR	Discharge count register	0x18	R	DCR7	DCR6	DCR5	DCR4	DCR3	DCR2	DCR1	DCR0
FLAGS3	Third status flags	0x4c	R	RSVD	RSVD	RSVD	RSVD	VQ	CR1	CR0	RSVD

APPLICATION INFORMATION

bq2016 applications schematic



PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ2016DBQ	NRND	SSOP	DBQ	28	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2016 E412	
BQ2016DBQG4	NRND	SSOP	DBQ	28	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	2016 E412	

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ACTIVE: Product device recommended for new designs.
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PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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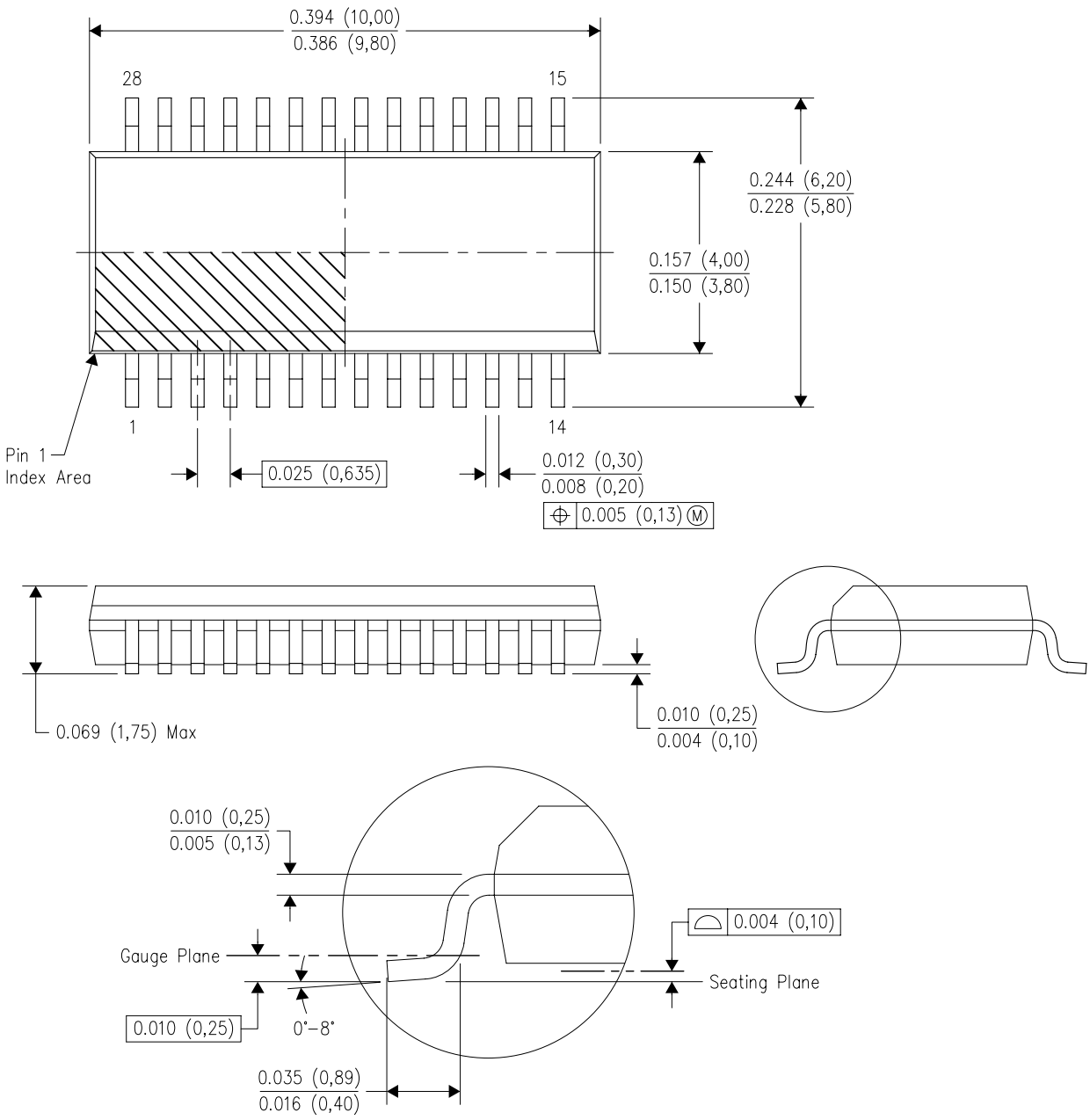
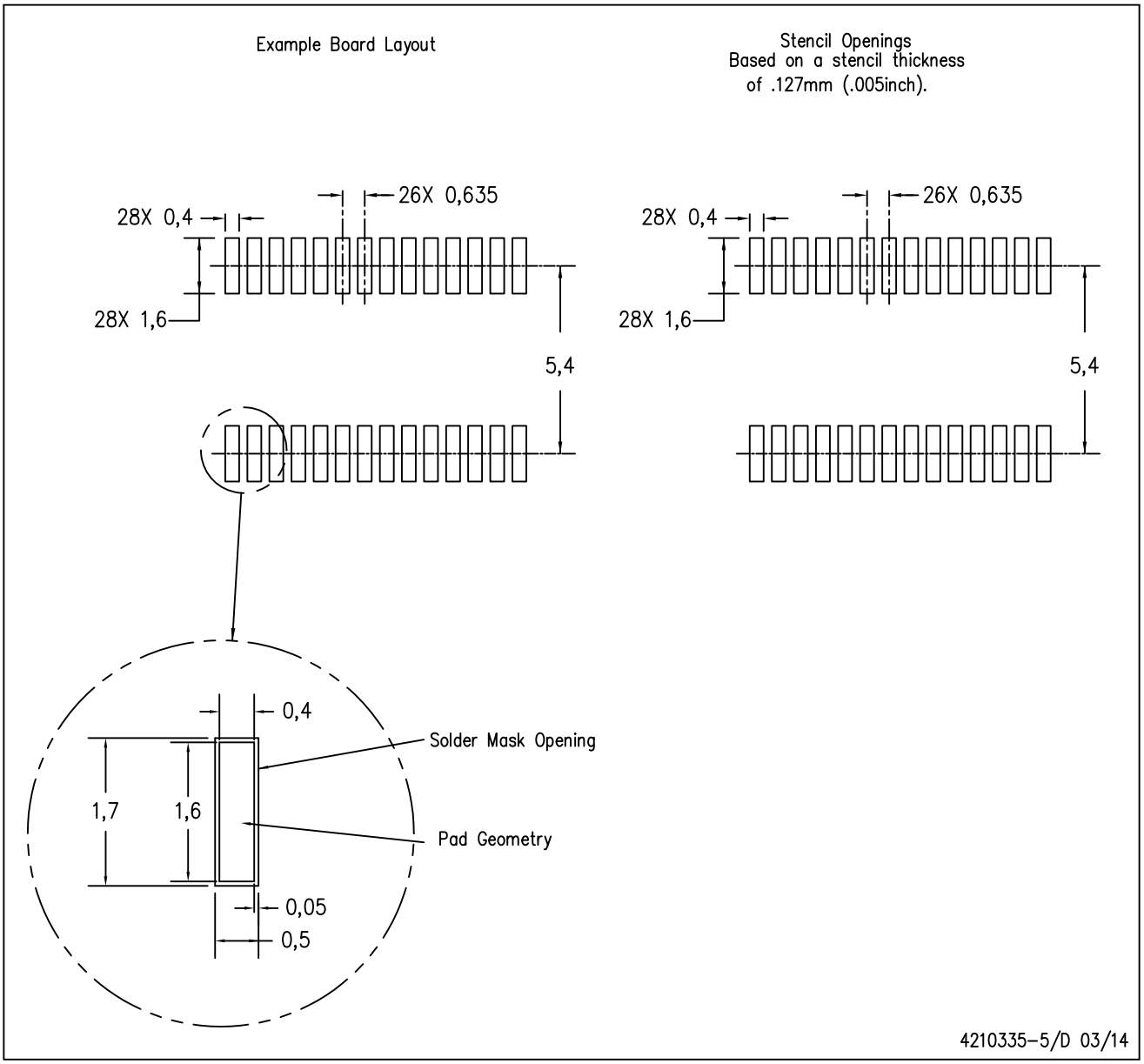
DBQ (R–PDSO–G28) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
D. Falls within JEDEC MO–137 variation AF.

DBQ (R–PDSO–G28) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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