lm392-N Low Power Operational Amplifier/Voltage Comparator

Check for Samples: LM392-N

FEATURES

- **Wide Power Supply Voltage Range**
  - **Single Supply: 3V to 32V**
  - **Dual Supply: ±1.5V to ±16V**
- **Low Supply Current Drain—Essentially Independent of Supply Voltage: 600 µA**
- **Low Input Biasing Current: 50 nA**
- **Low Input Offset Voltage: 2 mV**
- **Low Input Offset Current: 5 nA**
- **Input Common-Mode Voltage Range Includes Ground**
- **Differential Input Voltage Range Equal to the Power Supply Voltage**
- **ADDITIONAL OP AMP FEATURES**
  - **Internally Frequency Compensated for Unity Gain**
  - **Large DC Voltage Gain: 100 dB**
  - **Wide Bandwidth (Unity Gain): 1 MHz**
  - **Large Output Voltage Swing: 0V to V^+ − 1.5V**
- **ADDITIONAL COMPARATOR FEATURES**
  - **Low Output Saturation Voltage: 250 mV at 4 mA**
  - **Output Voltage Compatible with all Types of Logic Systems**

ADVANTAGES

- **Eliminates Need for Dual Power Supplies**
- **An Internally Compensated Op Amp and a Precision Comparator in the Same Package**
- **Allows Sensing at or Near Ground**
- **Power Drain Suitable for Battery Operation**
- **Pin-Out is the Same as Both the LM358 Dual Op Amp and the LM393 Dual Comparator**

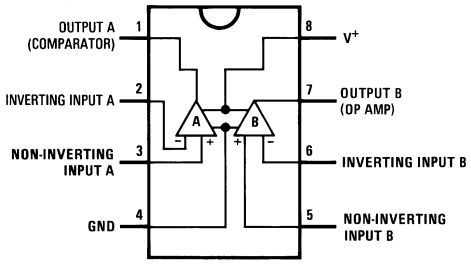
DESCRIPTION

The lm392-N series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the lm392-N extremely useful in the design of portable equipment.

Connection Diagram

Top View



(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

Figure 1. SOIC and PDIP Packages
See Package Numbers D0008A and P0008E

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

	lm392-N
Supply Voltage, V^+	32V or ±16V
Differential Input Voltage	32V
Input Voltage	−0.3V to +32V
Power Dissipation (3)	
Molded DIP (LM392N)	820 mW
Small Outline Package (LM392M)	530 mW
Output Short-Circuit to Ground (4)	Continuous
Input Current (V_{IN} < −0.3 V_{DC}) (5)	50 mA
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	260°C
ESD rating to be determined.	
Soldering Information	
Dual-in-Line Package	
Soldering (10 seconds)	260°C
Small Outline Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

(1) "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not ensure specific performance limits.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(3) For operating at temperatures above 25°C, the lm392-N must be derated based on a 125°C maximum junction temperature and a thermal resistance of 122°C/W which applies for the device soldered in a printed circuit board, operating in still air ambient. The dissipation is the total of both amplifiers—use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.
(4) Short circuits from the output to V^+ can cause excessive heating and eventual destruction. When considering short circuits to ground, the maximum output current is approximately 40 mA for the op amp and 30 mA for the comparator independent of the magnitude of V^+. At values of supply voltage in excess of 15V, continuous short circuits can exceed the power dissipation ratings and cause eventual destruction.
(5) This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the amplifiers to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than −0.3V (at 25°C).

Electrical Characteristics

(V^+ = 5 V_{DC}; specifications apply to both amplifiers unless otherwise stated) (1)

Parameter	Conditions	lm392-N			Units
		Min	Typ	Max	
Input Offset Voltage	T_A = 25°C, (2)		±2	±5	mV
Input Bias Current	IN(+) or IN(−), T_A =25°C, (3) , V_{CM} = 0V		50	250	nA
Input Offset Current	IN(+) − IN(−), T_A = 25°C		±5	±50	nA
Input Common-Mode Voltage Range	V^+ = 30 V_{DC}, T_A = 25°C, (4)	0		V^+−1.5	V
Supply Current	R_L = ∞ , V^+= 30 V		1	2	mA
Supply Current	R_L = ∞ , V^+= 5 V		0.5	1	mA

(1) These specifications apply for V^+ = 5V, unless otherwise stated. For the lm392-N, temperature specifications are limited to 0°C ≤ T_A ≤ +70°C.
(2) At output switch point, V_O ≅ 1.4V, R_S = 0Ω with V^+ from 5V to 30V; and over the full input common-mode range (0V to V^+ − 1.5V).
(3) The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.
(4) The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ − 1.5V, but either or both inputs can go to 32V without damage.

Electrical Characteristics (continued)

(V^+ = 5 V_{DC}; specifications apply to both amplifiers unless otherwise stated) (1)

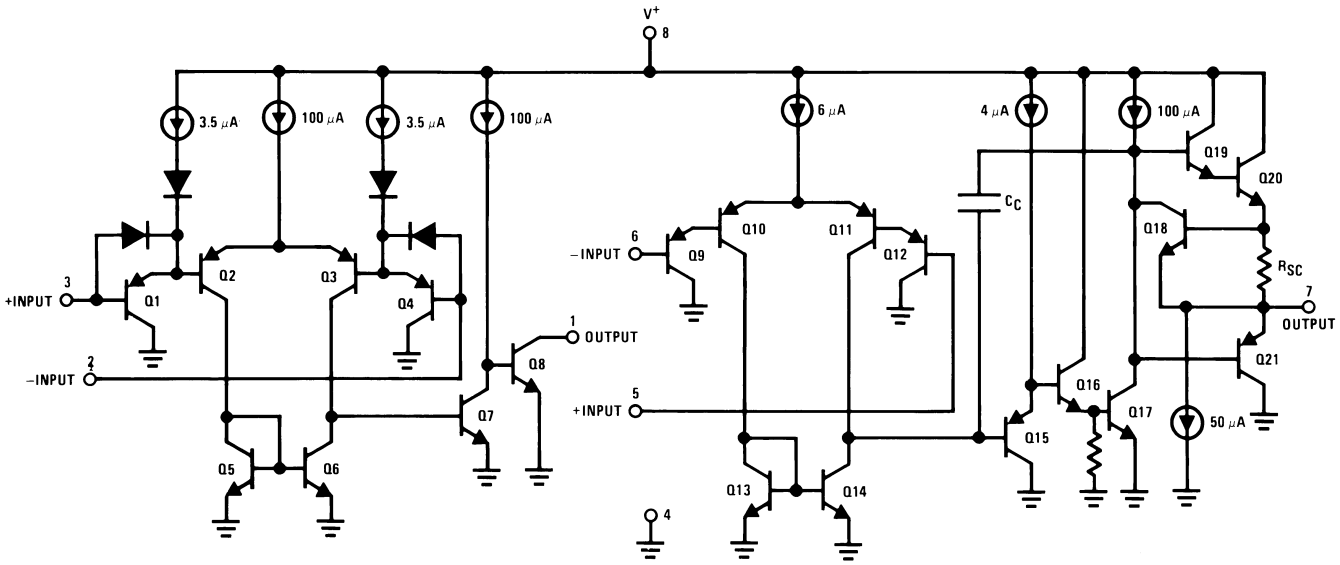
Parameter	Conditions	lm392-N			Units
		Min	Typ	Max	
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, T_A = 25°C, Input Referred, (5)		−100		dB
Input Offset Voltage	(2)			±7	mV
Input Bias Current	IN(+) or IN(−)			400	nA
Input Offset Current	IN(+) − IN(−)			150	nA
Input Common-Mode Voltage Range	V^+ = 30 V_{DC}, (4)	0		V^+−2	V
Differential Input Voltage	Keep All V_{IN}'s ≥ 0 V_{DC} (or V^-, if used) (6)			32	V
OP AMP ONLY					
Large Signal Voltage Gain	V^+ = 15 V_{DC}, V_o swing = 1 V_{DC} to 11 V_{DC}, R_L = 2 kΩ, T_A = 25°C	25	100		V/mV
Output Voltage Swing	R_L = 2 kΩ, T_A = 25°C	0		V^+−1.5	V
Common-Mode Rejection Ratio	DC, T_A = 25°C, V_{CM}= 0, V_{DC} to V^+−1.5 V_{DC}	65	70		dB
Power Supply Rejection Ratio	DC, T_A = 25°C	65	100		dB
Output Current Source	$V_{IN(+)}$ = 1 V_{DC}, $V_{IN(−)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o = 2 V_{DC}, T_A = 25°C	20	40		mA
Output Current Sink	$V_{IN(−)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =2V_{DC}, T_A = 25°C	10	20		mA
	$V_{IN(−)}$ = 1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V^+ = 15 V_{DC}, V_o =200 mV, T_A = 25°C	12	50		µA
Input Offset Voltage Drift	R_S = 0Ω		7		µV/°C
Input Offset Current Drift	R_S = 0Ω		10		pA_{DC}/°C
COMPARATOR ONLY					
Voltage Gain	R_L ≥ 15 kΩ, V^+ = 15 V_{DC}, T_A = 25°C	50	200		V/mV
Large Signal Response Time (7)	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC} V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		300		ns
Response Time	V_{RL} = 5 V_{DC}, R_L = 5.1 kΩ, T_A = 25°C		1.3		µs
Output Sink Current	$V_{IN(−)}$ =1 V_{DC}, $V_{IN(+)}$ = 0 V_{DC}, V_O ≥1.5 V_{DC}, T_A = 25°C	6	16		mA
Saturation Voltage	$V_{IN(−)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA, T_A = 25°C		250	400	mV
	$V_{IN(−)}$ ≥ 1 V_{DC}, $V_{IN(+)}$ = 0, I_{SINK} ≤ 4 mA			700	mV
Output Leakage Current	$V_{IN(−)}$ = 0, $V_{IN(+)}$ ≥ 1 V_{DC}, V_o = 5 V_{DC}, T_A = 25°C		0.1		nA
	$V_{IN(−)}$ = 0, $V_{IN(+)}$ ≥ 1 V_{DC}, V_o = 30 V_{DC}			1.0	µA

(5) Due to proximity of external components, insure that coupling is not originating via the stray capacitance between these external parts. This typically can be detected as this type of capacitive coupling increases at higher frequencies.

(6) Positive excursions of input voltage may exceed the power supply level. As long as the other input voltage remains within the common-mode range, the comparator will provide a proper output state. The input voltage to the op amp should not exceed the power supply level. The input voltage state must not be less than −0.3V (or 0.3V below the magnitude of the negative power supply, if used) on either amplifier.

(7) The response time specified is for a 100 mV input step with 5 mV overdrive. For larger overdrive signals 300 ns can be obtained.

Schematic Diagram



Comparator A Amplifier B

APPLICATION HINTS

Please refer to the application hints section of the LM193 and the LM158 datasheets.

REVISION HISTORY

Changes from Revision C (March 2013) to Revision D	Page
• Changed layout of National Data Sheet to TI format	6

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM392M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 70	LM392 M	
LM392M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM392 M	Samples
LM392MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 70	LM392 M	Samples
LM392N/NOPB	ACTIVE	PDIP	P	8	40	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	0 to 70	LM 392N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

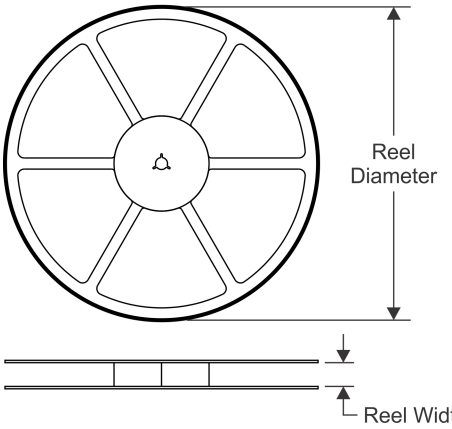
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

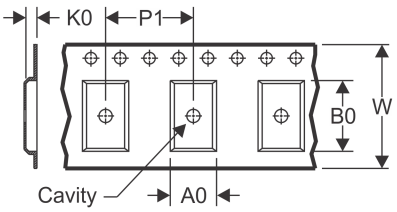
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

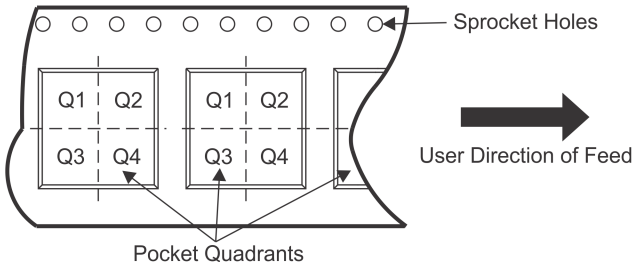


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

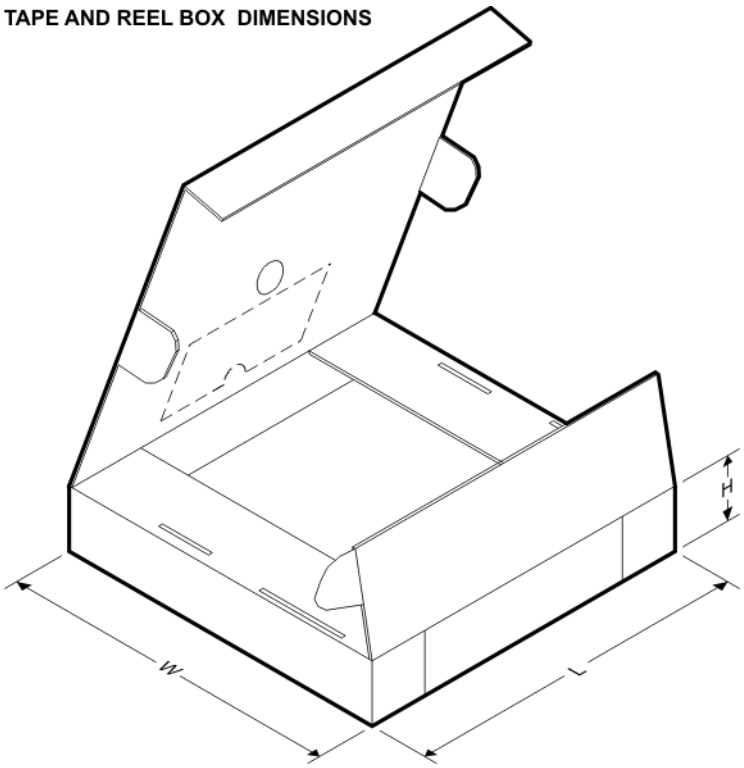
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM392MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

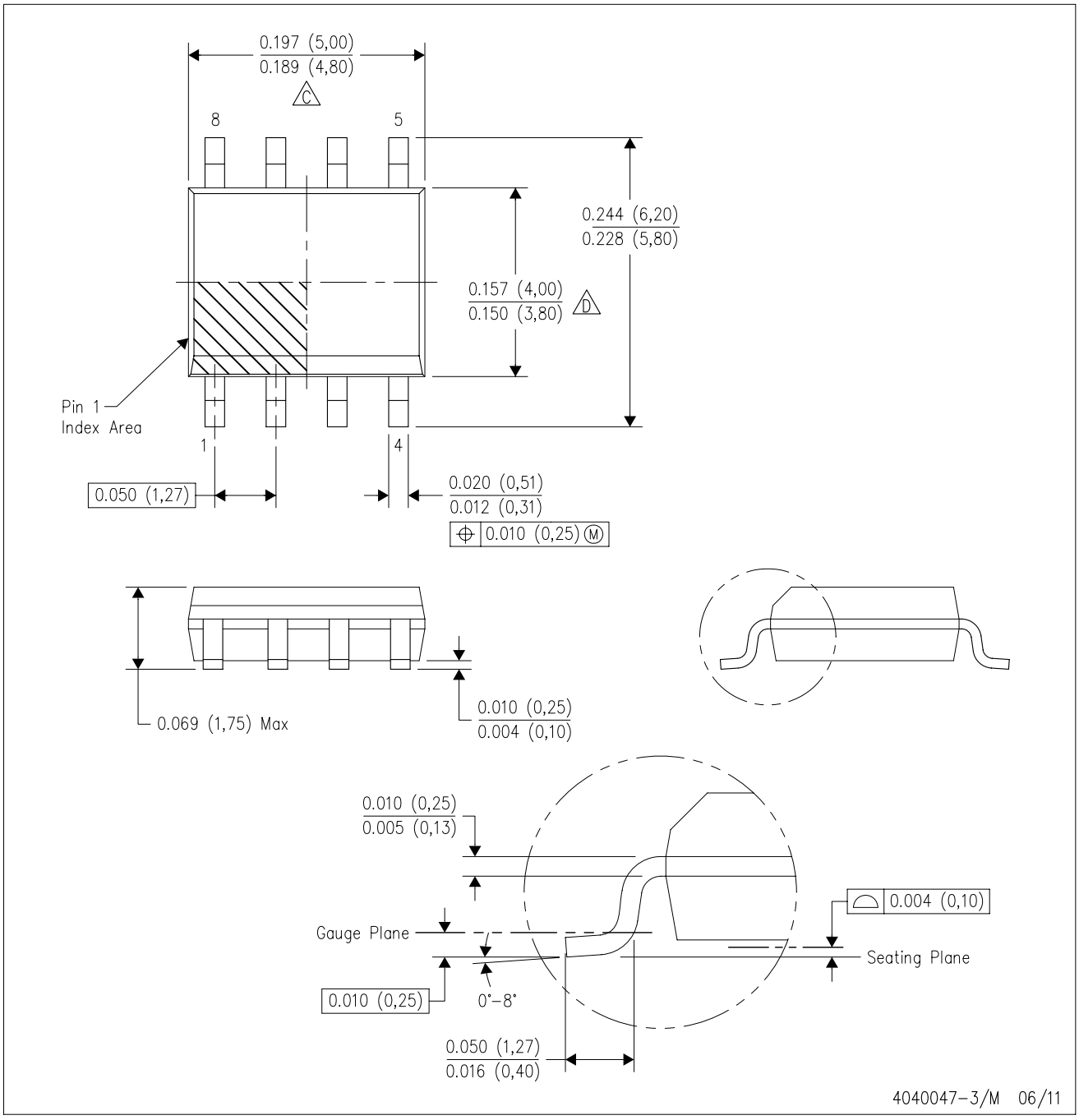
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

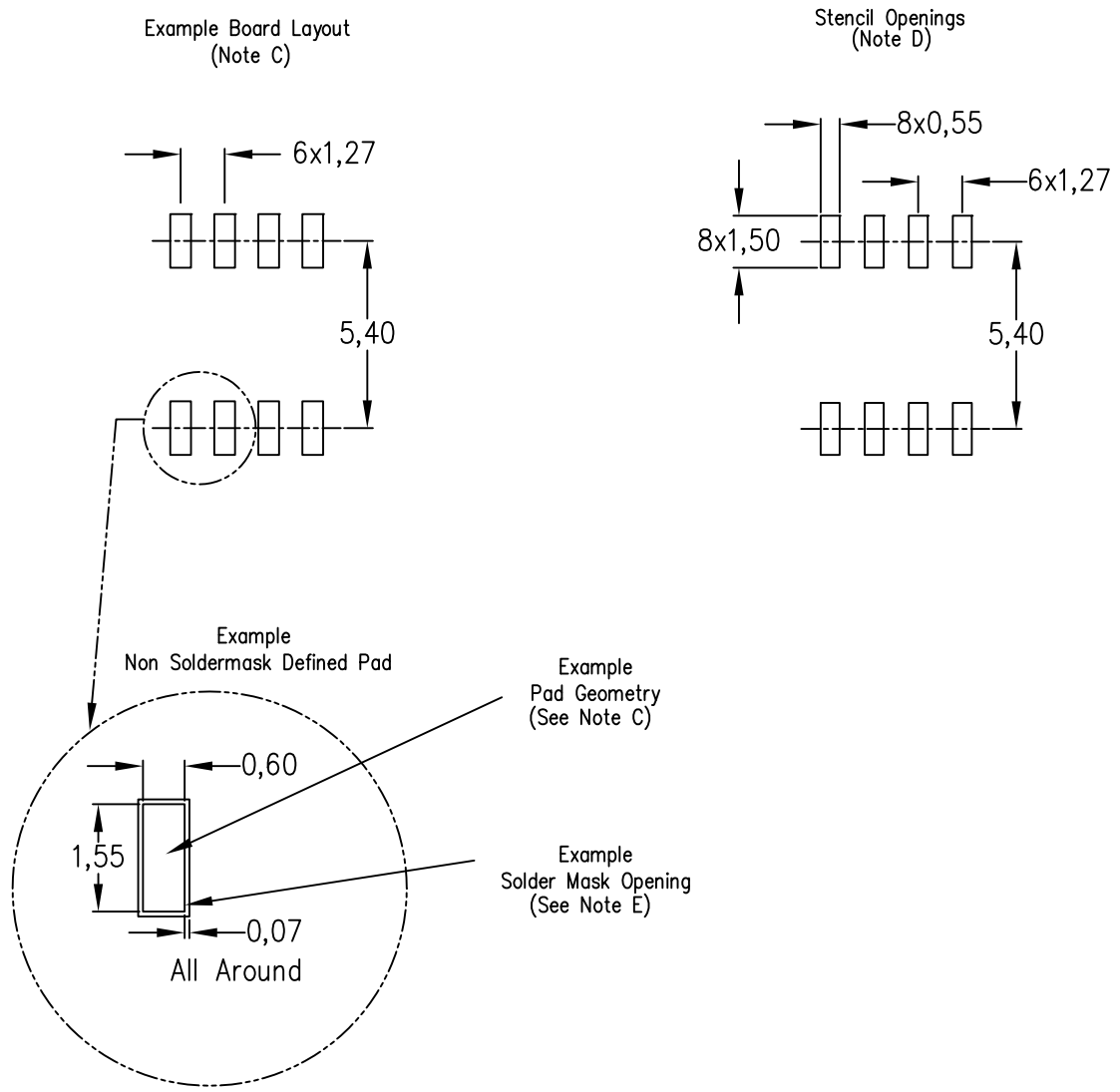
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM392MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



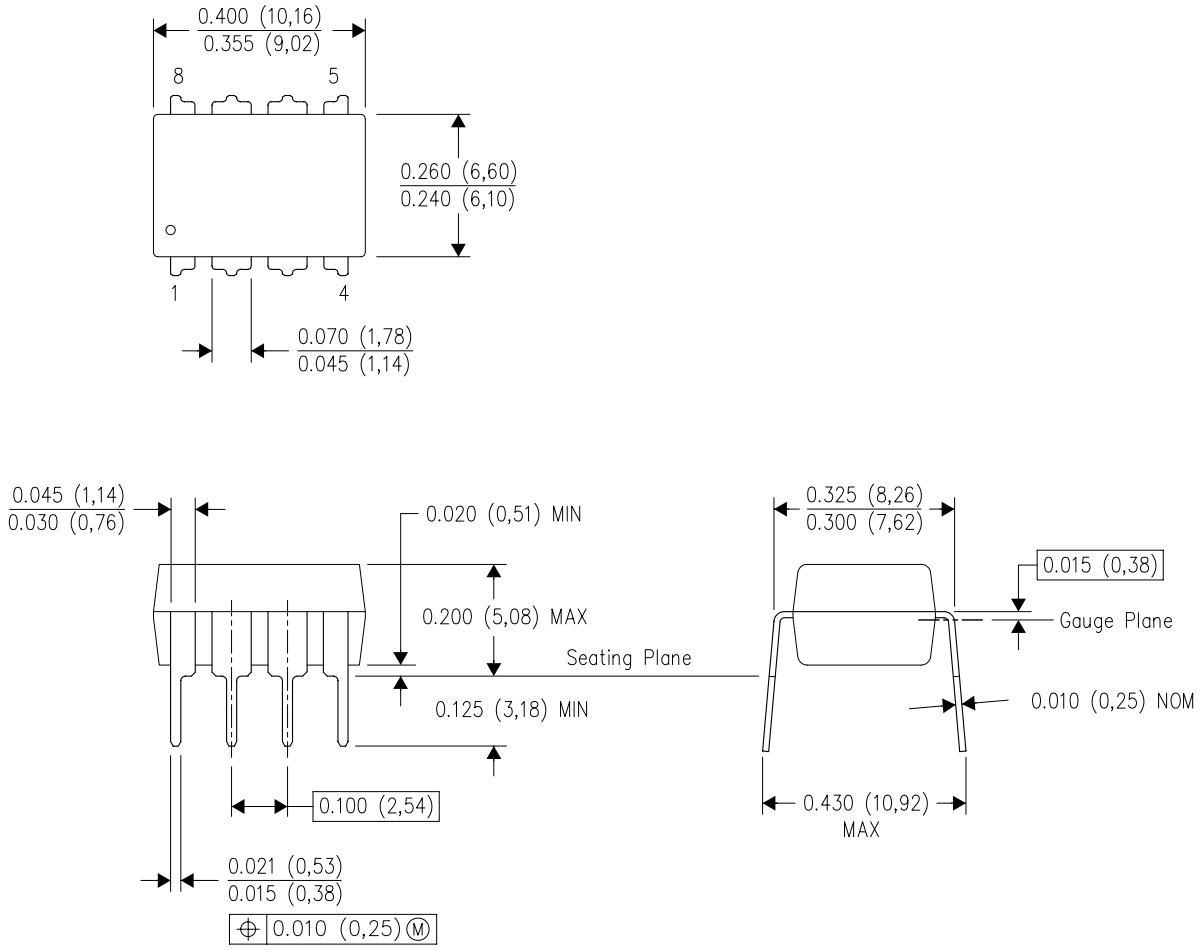
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

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