

## OPAx132 High-Speed FET-Input Operational Amplifiers

### 1 Features

- FET input:  $I_B = 50$  pA Maximum
- Wide Bandwidth: 8 MHz
- High Slew Rate: 20 V/ $\mu$ s
- Low Noise:  $8\text{ nV}/\sqrt{\text{Hz}}$  (1 kHz)
- Low Distortion: 0.00008%
- High Open-loop Gain: 130 dB (600- $\Omega$  load)
- Wide Supply Range:  $\pm 2.5$  to  $\pm 18$ V
- Low Offset Voltage: 500  $\mu$ V Maximum
- Single, Dual, and Quad Versions

### 2 Applications

- SAR ADC Driver
- Voltage Reference Buffer
- Trans-impedance Amplifier
- Photodiode Amplifier
- Active Filters
- Integrators

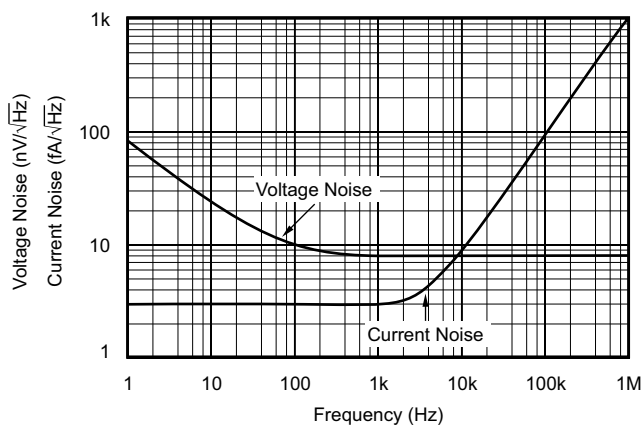
### 3 Description

The OPAx132 series of FET-input operational amplifiers provides highspeed and excellent DC performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

The OPAx132 operational amplifiers are easy to use and free from phase inversion and overload problems often found in common FET-input operational amplifiers. Input cascode circuitry provides excellent common-mode rejection and maintains low input bias current over its wide input voltage range. The OPAx132 series of operational amplifiers are stable in unity gain and provide excellent dynamic behavior over a wide range of load conditions, including high load capacitance. Dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

Single and dual versions are available in 8-pin DIP and SO-8 surface-mount packages. Quad is available in 14-pin DIP and SO-14 surface-mount packages. All are specified for  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  operation

Low Noise JFET Input



Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
OPAx132	PDIP (8) (P)	9.81 mm × 6.35 mm
	SOIC (8) (D)	4.90 mm × 3.91 mm
OPA2132	PDIP (8) (P)	9.81 mm × 6.35 mm
	SOIC (8) (D)	4.90 mm × 3.91 mm
OPA4132	PDIP (14) (N)	19.30 mm × 6.35 mm
	SOIC (14) (D)	8.65 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	8.1 Application Information.....	11
<b>3 Description</b> .....	<b>1</b>	8.2 Typical Application .....	12
<b>4 Revision History</b> .....	<b>2</b>	<b>9 Power Supply Recommendations</b> .....	<b>14</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Layout</b> .....	<b>14</b>
<b>6 Specifications</b> .....	<b>4</b>	10.1 Layout Guidelines .....	14
6.1 Absolute Maximum Ratings .....	4	10.2 Layout Example .....	15
6.2 ESD Ratings.....	4	<b>11 Device and Documentation Support</b> .....	<b>16</b>
6.3 Recommended Operating Conditions.....	4	11.1 Device Support .....	16
6.4 Electrical Characteristics.....	5	11.2 Documentation Support .....	16
6.5 Typical Characteristics .....	7	11.3 Related Links .....	16
<b>7 Detailed Description</b> .....	<b>10</b>	11.4 Trademarks .....	16
7.1 Overview .....	10	11.5 Electrostatic Discharge Caution.....	17
7.2 Functional Block Diagram .....	10	11.6 Glossary .....	17
7.3 Feature Description.....	10	<b>12 Mechanical, Packaging, and Orderable</b>	
7.4 Device Functional Modes.....	10	<b>Information</b> .....	<b>17</b>

## 4 Revision History

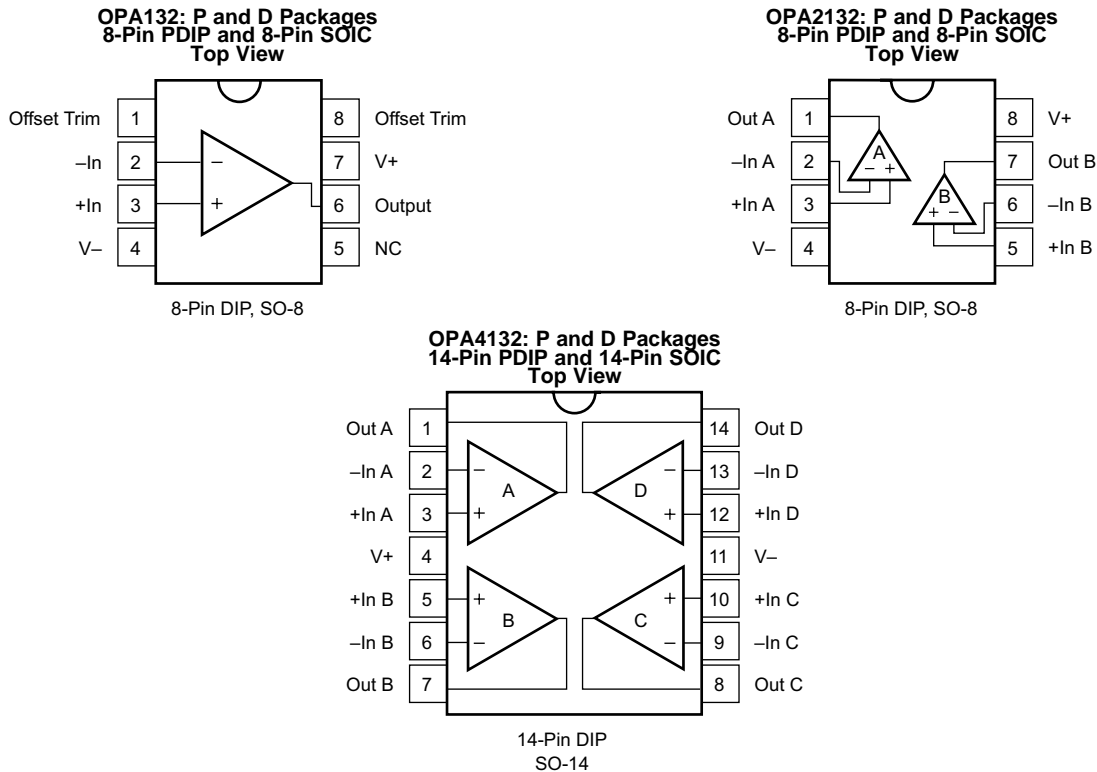
NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

### Changes from Revision A (June 2004) to Revision B

Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ..... **1**

## 5 Pin Configuration and Functions



### Pin Functions OPA132

PIN		I/O	DESCRIPTION
NAME	NO.		
Offset Trim	1	I	Input offset voltage adjust
-In	2	I	Inverting input
+In	3	I	Noninverting input
V-	4	—	Negative power supply
NC	5	—	No internal connection. Can be left floating.
Output	6	O	Output
V+	7	—	Positive power supply
Offset Trim	8	I	Input offset voltage adjust

### Pin Functions OPA2132 and OPA4132

PIN			I/O	DESCRIPTION
NAME	OPA2132 NO.	OPA4132 NO.		
Out A	1	1	O	Output channel A
-In A	2	2	I	Inverting input channel A
+In A	3	3	I	Noninverting input channel A
V+	8	4	—	Positive power supply
+In B	5	5	I	Noninverting input channel B
-In B	6	6	I	Inverting input channel B
Out B	7	7	O	Output channel B
Out C	—	8	O	Output channel C
-In C	—	9	I	Inverting input channel C

**Pin Functions OPA2132 and OPA4132 (continued)**

PIN			I/O	DESCRIPTION
NAME	OPA2132 NO.	OPA4132 NO.		
+In C	–	10	I	Noninverting input channel C
V–	4	11	—	Negative power supply
+In D	–	12	I	Noninverting input channel D
–In D	–	13	I	Inverting input channel D
Out D	–	14	O	Output channel D

## 6 Specifications

### 6.1 Absolute Maximum Ratings

 over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage, V+ to V–		36	V
Input voltage	(V–) –0.7	(V+) +0.7	V
Output short-circuit <sup>(2)</sup>	Continuous		
Operation temperature	–40	125	°C
Junction temperature		150	°C
T <sub>stg</sub> Storage temperature	–55	125	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Short-circuit to ground, one amplifier per package.

### 6.2 ESD Ratings

			VALUE	UNIT
<b>OPA132 in PDIP and SOIC Package, OPA2132 and OPA4132 in PDIP Package</b>				
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±2000	V
<b>OPA2132 in SOIC Package</b>				
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±500	
<b>OPA4132 in SOIC Package</b>				
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>		±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>		±200	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V <sub>S</sub> Supply voltage, V <sub>S</sub> = (V+) – (V–)	±2.5	±15	±18	V
T <sub>A</sub> Specified temperature range	–40		85	°C

## 6.4 Electrical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	OPAx132P, U OPA2132P, U			OPAx132PA, UA OPA2132PA, UA OPA4132PA, UA			UNIT	
		MIN	TYP	MAX	MIN	TYP	MAX		
<b>OFFSET VOLTAGE</b>									
Input Offset Voltage			$\pm 0.25$	$\pm 0.5$		$\pm 0.5$	$\pm 2$	mV	
vs Temperature <sup>(1)</sup>	Operating temperature range		$\pm 2$	$\pm 10$		$\pm 2$	$\pm 10$	$\mu\text{V}/^\circ\text{C}$	
vs Power Supply	$V_S = \pm 2.5\text{ V}$ to $\pm 18\text{ V}$		5	15		5	30	$\mu\text{V}/\text{V}$	
Channel Separation (dual and quad)	$R_L = 2\text{ k}\Omega$		0.2			0.2		$\mu\text{V}/\text{V}$	
<b>INPUT BIAS CURRENT</b>									
Input Bias Current <sup>(2)</sup>	$V_{CM} = 0\text{ V}$		5	$\pm 50$		5	$\pm 50$	pA	
vs Temperature			See Figure 5			See Figure 5			
Input Offset Current <sup>(2)</sup>	$V_{CM} = 0\text{ V}$		$\pm 2$	$\pm 50$		$\pm 2$	$\pm 50$	pA	
<b>NOISE</b>									
Input Voltage Noise									
Noise Density	f = 10 Hz		23			23		nV/ $\sqrt{\text{Hz}}$	
	f = 100 H		10			10			
	f = 1 kHz		8			8			
	f = 10 kHz		8			8			
Current Noise Density,	f = 1 kHz		3			3		fA/ $\sqrt{\text{Hz}}$	
<b>INPUT VOLTAGE RANGE</b>									
Common-Mode Voltage Range			(V-) +2.5	$\pm 13$	(V+) -2.5	(V-) +2.5	$\pm 13$	(V+) -2.5	V
Common-Mode Rejection	$V_{CM} = -12.5\text{ V}$ to $12.5\text{ V}$		96	100		86	94	dB	
<b>INPUT IMPEDANCE</b>									
Differential			$10^{13} \parallel 2$			$10^{13} \parallel 2$		$\Omega \parallel \text{pF}$	
Common-Mode	$V_{CM} = -12.5\text{ V}$ to $12.5\text{ V}$		$10^{13} \parallel 6$			$10^{13} \parallel 6$		$\Omega \parallel \text{pF}$	
<b>OPEN-LOOP GAIN</b>									
Open-Loop Voltage Gain	$R_L = 10\text{ k}\Omega$ , $V_O = -14.5\text{ V}$ to $13.8\text{ V}$		110	120		104	120	dB	
	$R_L = 2\text{ k}\Omega$ , $V_O = -13.8\text{ V}$ to $13.5\text{ V}$		110	126		104	120		
	$R_L = 600\ \Omega$ , $V_O = -12.8\text{ V}$ to $12.5\text{ V}$		110	130		104	120		
<b>FREQUENCY RESPONSE</b>									
Gain-Bandwidth Product			8			8		MHz	
Slew Rate			$\pm 20$			$\pm 20$		V/ $\mu\text{s}$	
Settling Time:	0.1%	G = -1, 10 V Step, $C_L = 100\text{ pF}$	0.7			0.7		$\mu\text{s}$	
	0.01%	G = -1, 10 V Step, $C_L = 100\text{ pF}$	1			1		$\mu\text{s}$	
Overload Recovery Time	G = $\pm$		0.5			0.5		$\mu\text{s}$	
Total Harmonic Distortion + Noise	1 kHz, G = 1, $V_O = 3.5\text{ V}_{\text{rms}}$	$R_L = 2\text{ k}\Omega$	0.00008%			0.00008%			
		$R_L = 600\ \Omega$	0.00009%			0.00009%			

(1) Specified by wafer test.

(2) High-speed test at  $T_J = 25^\circ\text{C}$ .

**OPA132, OPA2132, OPA4132**

SBOS054B – JANUARY 1995 – REVISED SEPTEMBER 2015

[www.ti.com](http://www.ti.com)
**Electrical Characteristics (continued)**

 At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

PARAMETER		TEST CONDITIONS	OPAx132P, U OPAx2132P, U			OPAx132PA, UA OPAx2132PA, UA OPAx4132PA, UA			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
<b>OUTPUT</b>									
Voltage Output	Positive	$R_L = 10\text{ k}\Omega$	(V+)	(V+)		(V+)	(V+)		V
	Negative		-1.2	-0.9		-1.2	-0.9		
	Positive	$R_L = 2\text{ k}\Omega$	(V-)	(V-)		(V-)	(V-)		
	Negative		+0.5	+0.3		+0.5	+0.3		
	Positive	$R_L = 600\ \Omega$	(V+)	(V+)		(V+)	(V+)		
	Negative		-1.5	-1.1		-1.5	-1.1		
			(V-)	(V-)		(V-)	(V-)		
			+1.2	+0.9		+1.2	+0.9		
Short-Circuit Current			$\pm 40$			$\pm 40$			mA
Capacitive Load Drive (Stable Operation)			See <a href="#">Figure 17</a>			See <a href="#">Figure 17</a>			
<b>POWER SUPPLY</b>									
Specified Operating Voltage			$\pm 15$			$\pm 15$			V
Operating Voltage Range			$\pm 2.5$			$\pm 18$			V
Quiescent Current (per amplifier)		$I_O = 0$	$\pm 4$			$\pm 4.8$			mA
<b>TEMPERATURE RANGE</b>									
Operating Range			-40			85			$^\circ\text{C}$
Storage			-40			125			$^\circ\text{C}$

### 6.5 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

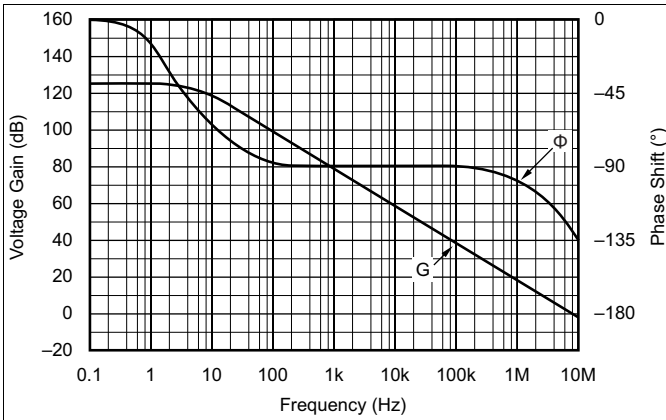


Figure 1. Open-Loop Gain and Phase vs Frequency

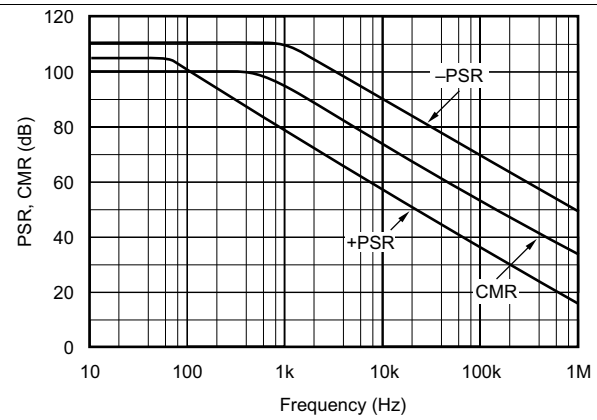


Figure 2. Power Supply and Common-Mode Rejection vs Frequency

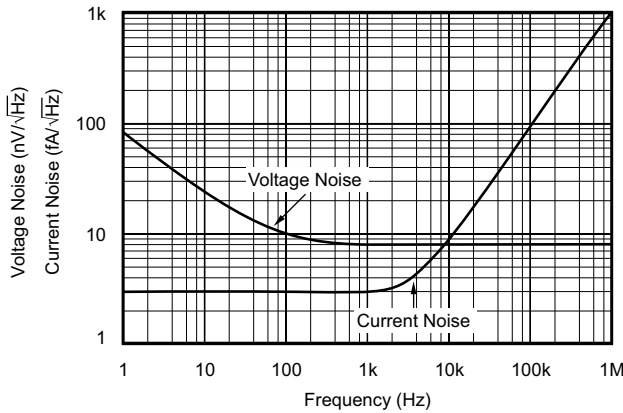


Figure 3. Input Voltage and Current Noise Spectral Density vs Frequency

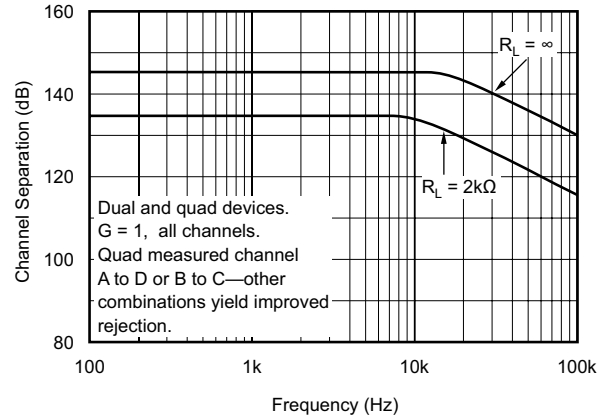


Figure 4. Channel Separation vs Frequency

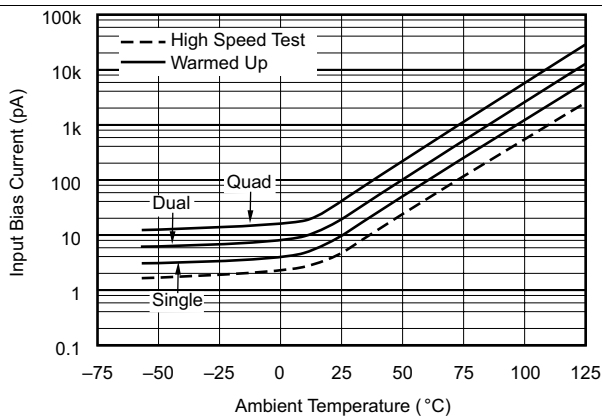


Figure 5. Input Bias Current vs Temperature

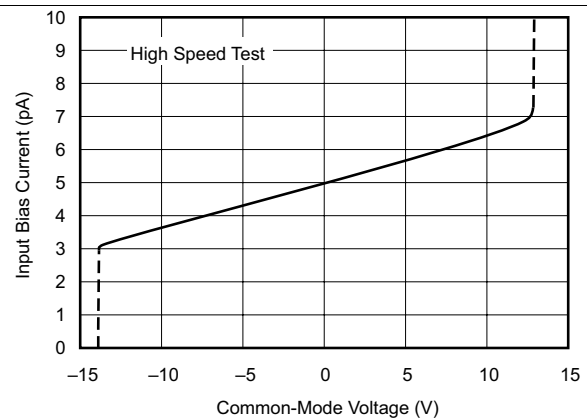


Figure 6. Input Bias Current vs Input Common-Mode Voltage

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.

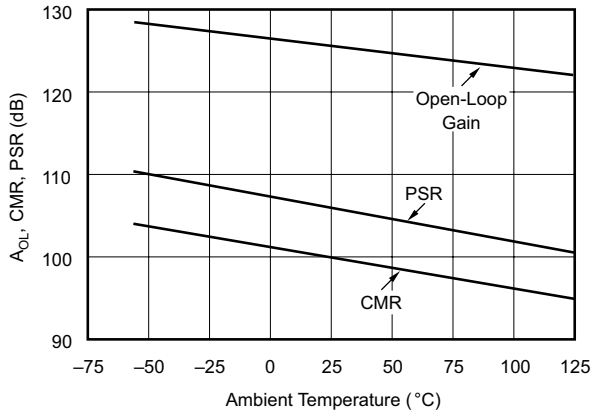


Figure 7.  $A_{OL}$ , CMR, PSR vs Temperature

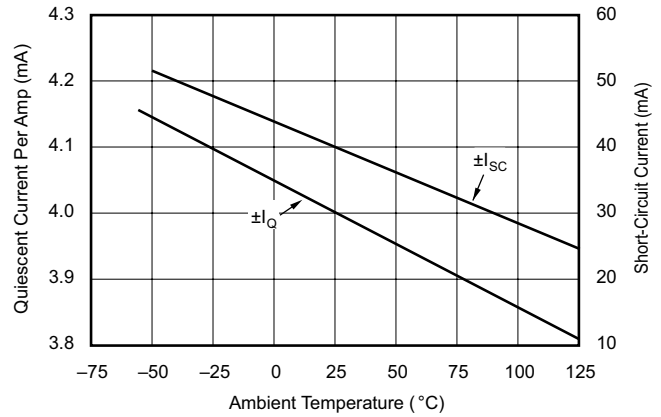


Figure 8. Quiescent Current and Short-Circuit Current vs Temperature

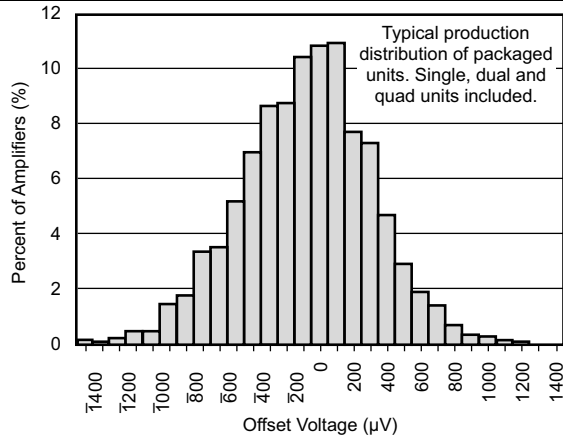


Figure 9. Offset Voltage Production Distribution

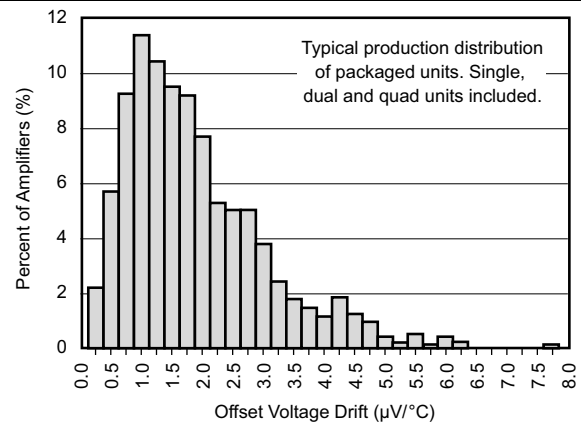


Figure 10. Offset Voltage Drift Production Distribution

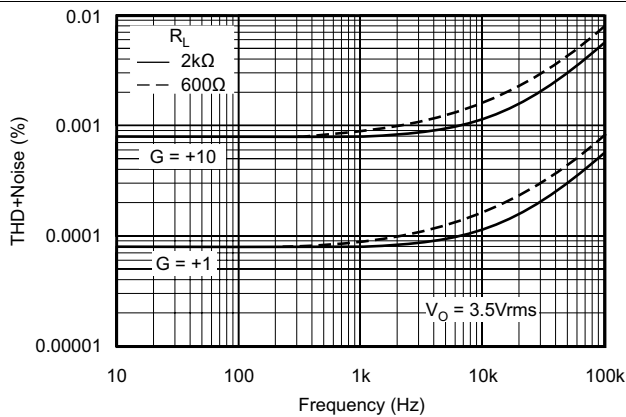


Figure 11. Total Harmonic Distortion + Noise vs Frequency

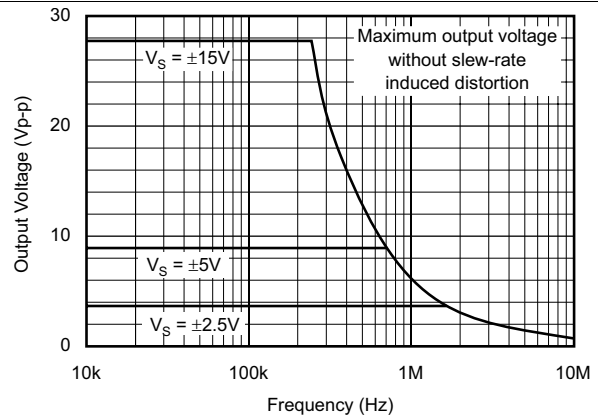
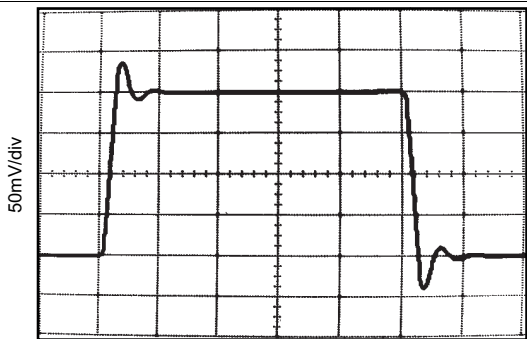


Figure 12. Maximum Output Voltage vs Frequency



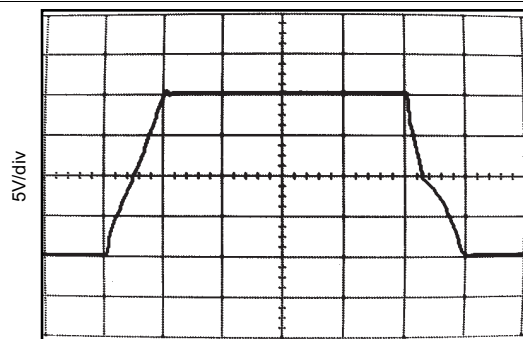
Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ ,  $R_L = 2\text{ k}\Omega$ , unless otherwise noted.



$G = 1$   
 $C_L = 100\text{pF}$

Figure 13. Small-Signal Step Response



$G = 1$   
 $C_L = 100\text{pF}$

Figure 14. Large-Signal Step Response

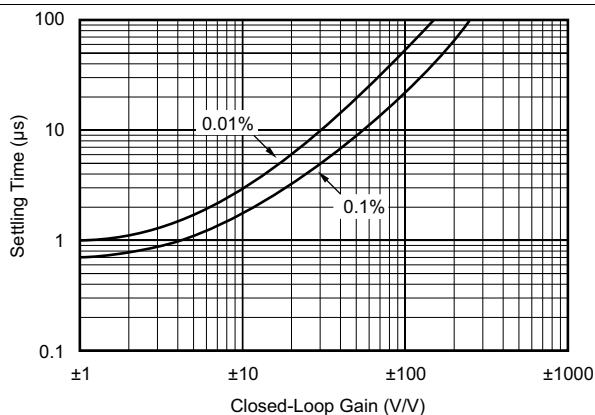


Figure 15. Settling Time vs Closed-Loop Gain

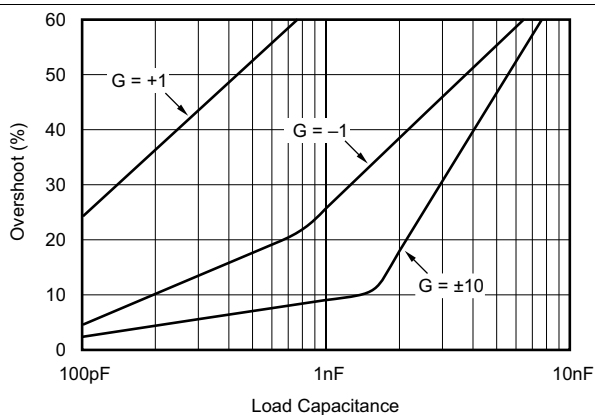


Figure 16. Small-Signal Overshoot vs Load Capacitance

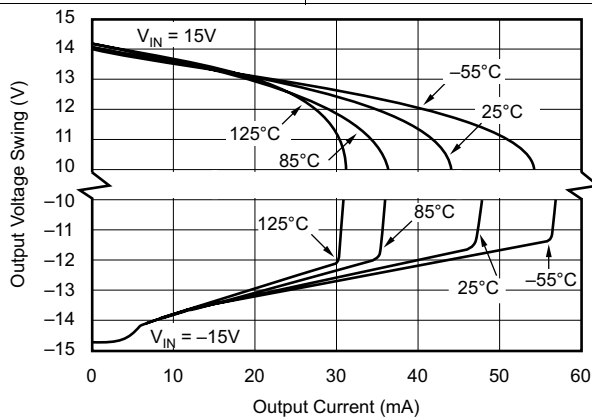


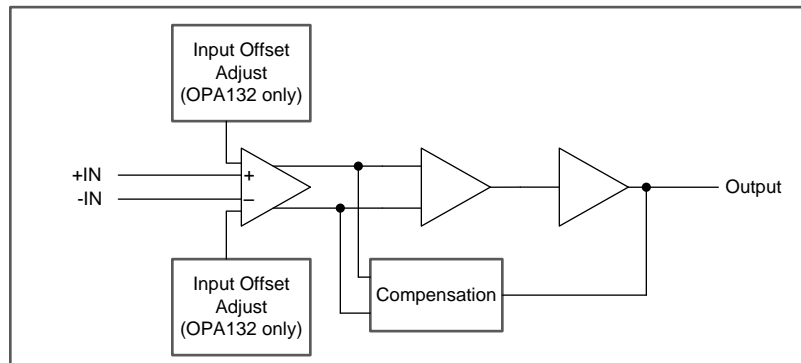
Figure 17. Output Voltage Swing vs Output Current

## 7 Detailed Description

### 7.1 Overview

The OPAx132 series of FET-input operational amplifiers provides highspeed and excellent dc performance. The combination of high slew rate and wide bandwidth provide fast settling time. Single, dual, and quad versions have identical specifications for maximum design flexibility. High performance grades are available in the single and dual versions. All are ideal for general-purpose, audio, data acquisition and communications applications, especially where high source impedance is encountered.

### 7.2 Functional Block Diagram



### 7.3 Feature Description

The OPAx132 series of JFET operational amplifiers combine low noise and wide bandwidth with precision and low input bias current to make them the ideal choice for applications with a high source impedance. The OPAx132 is unity-gain stable and features high slew rate ( $\pm 20$  V/ $\mu$ s) and wide bandwidth (8 MHz).

### 7.4 Device Functional Modes

The OPAx132 has a single functional mode and is operational when the power-supply voltage is greater than 5 V ( $\pm 2.5$  V). The maximum power supply voltage for the OPAx132 is 36 V ( $\pm 18$  V).

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The OPAx132 series operational amplifiers are unity-gain stable and suitable for a wide range of general-purpose applications. Power supply pins should be bypassed with 10-nF ceramic capacitors or larger.

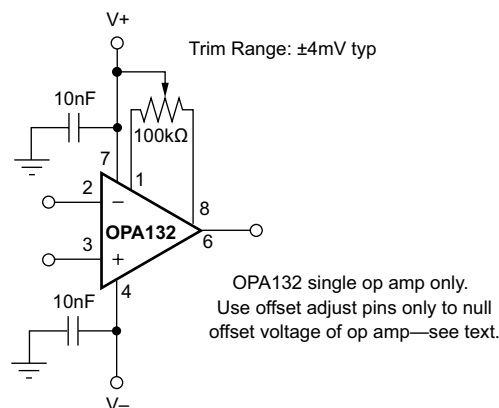
The OPAx132 series operational amplifiers are free from unexpected output phase reversal common with FET operational amplifiers. Many FET-input operational amplifiers exhibit phase-reversal of the output when the input common-mode voltage range is exceeded. This can occur in voltage-follower circuits, causing serious problems in control loop applications. The OPAx132 series of operational amplifiers are free from this undesirable behavior. All circuitry is completely independent in dual and quad versions, assuring normal behavior when one amplifier in a package is overdriven or short-circuited.

#### 8.1.1 Operating Voltage

The OPAx132 series of operation amplifiers operate with power supplies from  $\pm 2.5$  V to  $\pm 18$  V with excellent performance. Although specifications are production tested with  $\pm 15$  V supplies, most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage are shown in the [Typical Characteristics](#) section.

#### 8.1.2 Offset Voltage Trim

Offset voltage of the OPAx132 series of amplifiers is laser trimmed and usually requires no user adjustment. The OPAx132 amplifier (single op amp version) provides offset voltage trim connections on pins 1 and 8. Offset voltage can be adjusted by connecting a potentiometer as shown in [Figure 18](#). This adjustment should be used only to null the offset of the operational amplifier, not to adjust system offset or offset produced by the signal source. Nulling offset could degrade the offset voltage drift behavior of the operational amplifier. While it is not possible to predict the exact change in drift, the effect is usually small.



**Figure 18. OPAx132 Offset Voltage Trim Circuit**

#### 8.1.3 Input Bias Current

The FET-inputs of the OPAx132 series provide very low input bias current and cause negligible errors in most applications. For applications where low input bias current is crucial, junction temperature rise should be minimized. The input bias current of FET-input operational amplifiers increases with temperature as shown in [Figure 5](#).

The OPAx132 series may be operated at reduced power supply voltage to minimize power dissipation and temperature rise. Using  $\pm 3$  V supplies reduces power dissipation to one-fifth that at  $\pm 15$  V.

## Application Information (continued)

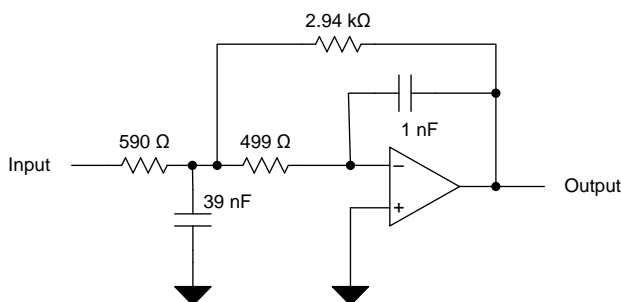
The dual and quad versions have higher total power dissipation than the single, leading to higher junction temperature. Thus, a warmed-up quad will have higher input bias current than a warmed-up single. Furthermore, an SOIC will generally have higher junction temperature than a DIP at the same ambient temperature because of a larger  $\theta_{JA}$ .

Printed-circuit-board layout can also help minimize junction temperature rise. Temperature rise can be minimized by soldering the devices to the circuit board rather than using a socket. Wide copper traces will also help dissipate the heat by acting as an additional heat sink.

Input stage cascode circuitry assures that the input bias current remains virtually unchanged throughout the full input common-mode range of the OPAx132 series. See [Figure 6](#).

## 8.2 Typical Application

The OPAx132 family offers outstanding dc precision and ac performance. These devices operate up to 36-V supply rails and offer ultralow input bias current and input bias current noise, as well as 8-MHz bandwidth and high capacitive load drive. These features make the OPAx132 a robust, high-performance operational amplifier for high-voltage industrial applications with high source impedance.



**Figure 19. OPA132 2nd Order 30 kHz, Low Pass Filter Schematic**

### 8.2.1 Design Requirements

Use the following parameters for this application:

- Gain = 5 V/V
- Low pass cutoff frequency = 30 kHz
- -40 db/dec filter response
- Maintain less than 3-dB gain peaking in the gain versus frequency response

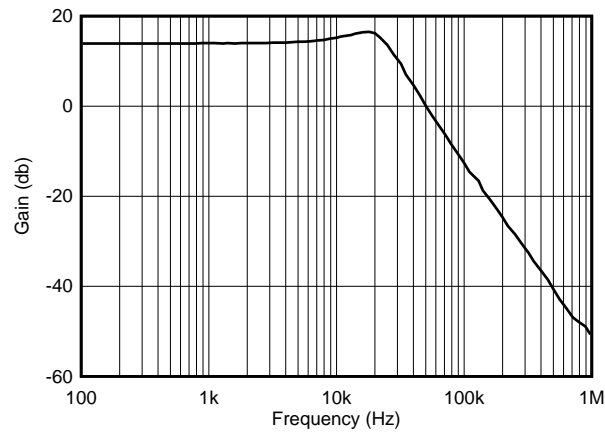
### 8.2.2 Detailed Design Procedure

[WEBENCH® Filter Designer](#) is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

Available as a web based tool from the WEBENCH® Design Center, [WEBENCH® Filter Designer](#) allows you to design, optimize, and simulate complete multistage active filter solutions within minutes.

**Typical Application (continued)**

**8.2.3 Application Curve**



**Figure 20. OPA132 2nd Order 30-kHz, Low Pass Filter Response**

## 9 Power Supply Recommendations

The OPAx132 is specified for operation from 5 V to 36 V ( $\pm 2.5$  V to  $\pm 18$  V); many specifications apply from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in the [Typical Characteristics](#).

### CAUTION

Supply voltages larger than 36 V can permanently damage the device; see the [Absolute Maximum Ratings](#).

Place 10-nF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the [Layout Guidelines](#).

## 10 Layout

### 10.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and operational amplifier itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 10 nF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. For more detailed information refer to *Circuit Board Layout Techniques*, [SLOA089](#).
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [Layout Example](#), keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at  $85^{\circ}\text{C}$  for 30 minutes is sufficient for most circumstances.

## 10.2 Layout Example

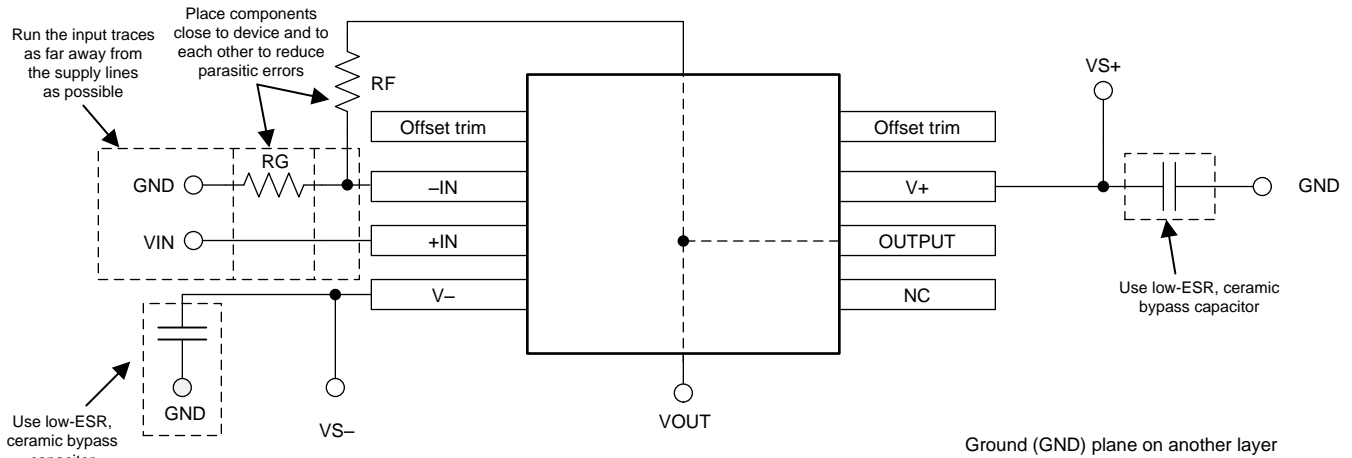
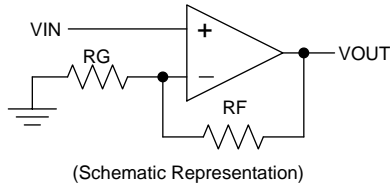


Figure 21. OPA132 Layout Example for the Noninverting Configuration

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Development Support

##### 11.1.1.1 WEBENCH Filter Designer Tool

**WEBENCH® Filter Designer** is a simple, powerful, and easy-to-use active filter design program. The WEBENCH Filter Designer lets you create optimized filter designs using a selection of TI operational amplifiers and passive components from TI's vendor partners.

##### 11.1.1.2 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a [free download](#) from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

#### NOTE

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).

##### 11.1.1.3 TI Precision Designs

The OPAx132 is featured in several TI Precision Designs, available online at <http://www.ti.com/ww/en/analog/precision-designs/>. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

### 11.2 Documentation Support

#### 11.2.1 Related Documentation

For related documentation, see the following:

- *EMI Rejection Ratio of Operational Amplifiers*, [SBOA128](#)
- *Circuit Board Layout Techniques*, [SLOA089](#)

### 11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
OPA132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA2132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
OPA4132	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.4 Trademarks

TINA-TI is a trademark of Texas Instruments.

TINA, DesignSoft are trademarks of DesignSoft, Inc.

All other trademarks are the property of their respective owners.



## 11.5 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	<a href="#">Samples</a>
OPA132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	<a href="#">Samples</a>
OPA132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 132U A	<a href="#">Samples</a>
OPA132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		OPA 132U	<a href="#">Samples</a>
OPA2132P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P	<a href="#">Samples</a>
OPA2132PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	<a href="#">Samples</a>
OPA2132PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		OPA2132P A	<a href="#">Samples</a>
OPA2132U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>
OPA2132U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2132U/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>
OPA2132U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>
OPA2132UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	<a href="#">Samples</a>
OPA2132UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	<a href="#">Samples</a>
OPA2132UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	<a href="#">Samples</a>
OPA2132UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	<a href="#">Samples</a>
OPA2132UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U A	<a href="#">Samples</a>
OPA2132UE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>
OPA2132UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	OPA 2132U	<a href="#">Samples</a>
OPA4132UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	<a href="#">Samples</a>
OPA4132UA/2K5	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	<a href="#">Samples</a>
OPA4132UA/2K5E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	<a href="#">Samples</a>
OPA4132UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU-DCC	Level-3-260C-168 HR	-40 to 85	OPA4132UA	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of  $\leq 1000$ ppm threshold. Antimony trioxide based flame retardants must also meet the  $\leq 1000$ ppm threshold requirement.

<sup>(3)</sup> **MSL, Peak Temp.** - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

<sup>(4)</sup> There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

<sup>(5)</sup> Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> **Lead/Ball Finish** - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2132UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4132UA/2K5	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA132U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2132U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA2132UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
OPA4132UA/2K5	SOIC	D	14	2500	367.0	367.0	38.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  -  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  -  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



4040047-3/M 06/11

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R-PDIP-T8)

PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

## IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make corrections, enhancements, improvements and other changes to its semiconductor products and services per JESD46, latest issue, and to discontinue any product or service per JESD48, latest issue. Buyers should obtain the latest relevant information before placing orders and should verify that such information is current and complete.

TI's published terms of sale for semiconductor products (<http://www.ti.com/sc/docs/stdterms.htm>) apply to the sale of packaged integrated circuit products that TI has qualified and released to market. Additional terms may apply to the use or sale of other types of TI products and services.

Reproduction of significant portions of TI information in TI data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. TI is not responsible or liable for such reproduced documentation. Information of third parties may be subject to additional restrictions. Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Buyers and others who are developing systems that incorporate TI products (collectively, "Designers") understand and agree that Designers remain responsible for using their independent analysis, evaluation and judgment in designing their applications and that Designers have full and exclusive responsibility to assure the safety of Designers' applications and compliance of their applications (and of all TI products used in or for Designers' applications) with all applicable regulations, laws and other applicable requirements. Designer represents that, with respect to their applications, Designer has all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. Designer agrees that prior to using or distributing any applications that include TI products, Designer will thoroughly test such applications and the functionality of such TI products as used in such applications.

TI's provision of technical, application or other design advice, quality characterization, reliability data or other services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using TI Resources in any way, Designer (individually or, if Designer is acting on behalf of a company, Designer's company) agrees to use any particular TI Resource solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

Designer is authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS. TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY DESIGNER AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

Unless TI has explicitly designated an individual product as meeting the requirements of a particular industry standard (e.g., ISO/TS 16949 and ISO 26262), TI is not responsible for any failure to meet such industry standard requirements.

Where TI specifically promotes products as facilitating functional safety or as compliant with industry functional safety standards, such products are intended to help enable customers to design and create their own applications that meet applicable functional safety standards and requirements. Using products in an application does not by itself establish any safety features in the application. Designers must ensure compliance with safety-related requirements and standards applicable to their applications. Designer may not use any TI products in life-critical medical equipment unless authorized officers of the parties have executed a special contract specifically governing such use. Life-critical medical equipment is medical equipment where failure of such equipment would cause serious bodily injury or death (e.g., life support, pacemakers, defibrillators, heart pumps, neurostimulators, and implantables). Such equipment includes, without limitation, all medical devices identified by the U.S. Food and Drug Administration as Class III devices and equivalent classifications outside the U.S.

TI may expressly designate certain products as completing a particular qualification (e.g., Q100, Military Grade, or Enhanced Product). Designers agree that it has the necessary expertise to select the product with the appropriate qualification designation for their applications and that proper product selection is at Designers' own risk. Designers are solely responsible for compliance with all legal and regulatory requirements in connection with such selection.

Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.