TPS727 250-mA, Ultralow I_Q, Fast Transient Response, RF Low-Dropout Linear Regulator

1 Features

- Very Low Dropout:
  - 65 mV Typical at 100 mA
  - 130 mV Typical at 200 mA
  - 163 mV Typical at 250 mA
- 2% Accuracy Over Load, Line, Temperature
- Ultralow I_Q: 7.9 µA
- Excellent Load Transient Performance:±50 mV for 200 mA Loading and Unloading Transient
- Available in Fixed-Output Voltages From 0.9 V to 5 V Using Innovative Factory EEPROM Programming
- High PSRR: 70 dB at 1 kHz
- Stable with a 1.0-µF Ceramic Capacitor
- Thermal Shutdown and Overcurrent Protection
- Available in 4-Ball, 0.4-mm Pitch Wafer-Level Chip Scale and 1.5-mm × 1.5-mm SON Packages

2 Applications

- Wireless Handsets, Smart Phones, PDAs
- MP3 Players and Other Handheld Products
- Wireless LAN, Bluetooth®, Zigbee®
- Remote Controls
- Portable Consumer Products

3 Description

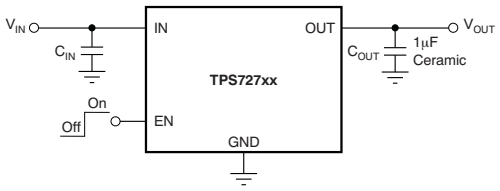
The TPS727 family of low-dropout (LDO) linear regulators are ultralow quiescent current LDOs with excellent line and ultra-fast load transient performance and are designed for power-sensitive applications. The LDO output voltage level is preset by the use of innovative factory EEPROM programming. A precision band-gap and error amplifier provides overall 2% accuracy over load, line, and temperature extremes. The TPS727 family is available in 1.5-mm × 1.5-mm SON and wafer chip-scale (WCSP) packages that make the devices ideal for handheld applications. This family of devices is fully specified over a temperature range of T_J = –40°C to +125°C.

Device Information

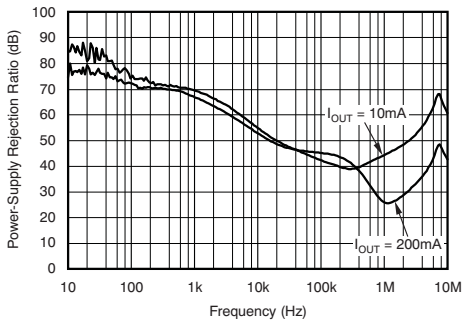
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS727xxDSE	WSON (6)	1.50 mm × 1.50 mm
TPS727xxYFF	DSBGA (4)	1.20 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

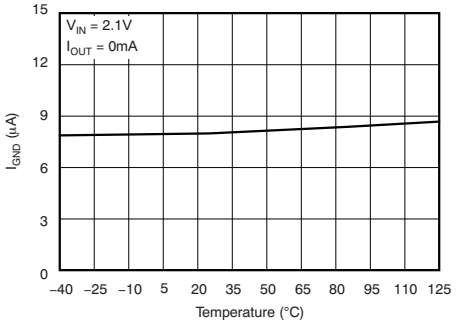
TYPICAL APPLICATION CIRCUIT



PSRR vs FREQUENCY



GROUND PIN CURRENT vs TEMPERATURE



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision E (September 2014) to Revision F — **Page**

- Changed DSBGA body size in *Device Information* table ... 1

Changes from Revision D (February 2014) to Revision E — **Page**

- Added TPS727105 to document ... 1
- Changed *terminal* to *pin* throughout document ... 1
- Updated Device Information table to current standards ... 1
- Changed Pin Configurations note ... 4
- Changed Pin Functions table: reordered table by pin name, added I/O column ... 4
- Updated Handling Ratings table to current standard ... 5
- Changed Thermal Information table: updated symbols ... 5
- Deleted *new generation* from first sentence of *Overview* section ... 11
- Added note to *Applications and Implementation* section ... 13

Changes from Revision C (January, 2011) to Revision D — **Page**

- Changed format to meet latest data sheet standards; added new sections and moved existing sections ... 1
- Deleted pinout diagrams from front page; see *Pin Configurations and Functions* section. ... 1
- Changed Pin Configurations section and moved to Pin Configurations and Functions section ... 4
- Changed note in Pin Configurations and Functions section. ... 4
- Deleted Figure 26 and Figure 27 ... 17

Changes from Revision B (April, 2010) to Revision C — **Page**

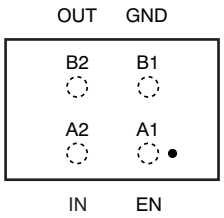
- Updated YFF front page pin drawing to show pin locations ... 1
- Revised Pin Configurations section ... 4
- Changed graph title for Figure 6 ... 7

Changes from Revision A (September, 2009) to Revision B **Page**

- Updated *Features* list 1
- Changed title of data sheet..... 1
- Changed footnote 2 to *Absolute Maximum Ratings* table 5
- Revised numerous specifications and parameters in *Electrical Characteristics* table 6
- Revised operating parameters for Figure 4..... 7
- Replaced Figure 5 7
- Added operating parameters to Figure 6..... 7
- Updated Figure 9..... 7

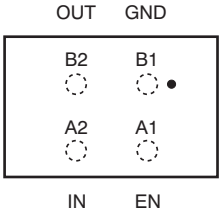
5 Pin Configurations and Functions

TPS72715, TPS72718, TPS72728, TPS72748
YFF Package
DSBGA-4
Top View



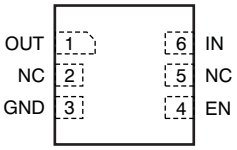
See note.

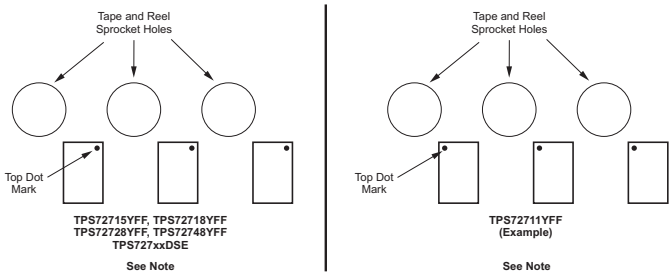
All Other TPS727 Devices
YFF Package
DSBGA-4
Top View



See note.

DSE Package
1,5mm × 1,5mm WSON-6
Top View





NOTE

The **EN** pin is marked with a dot for the 1.5-V, 1.8-V, 2.8-V, and 4.8-V versions of the YFF package. The **GND** pin is marked with a dot for all other voltage versions of the YFF package. Refer to YFF0004 Package Outline page included at the end of this document for dimensions of the YFF package. On the package outline, the shaded box indicates the location of ball A1 and does not correlate to any marking on the topside of the physical package.

Pin Functions

PIN			I/O	DESCRIPTION
NAME	YFF	DSE		
EN	A1	4	I	Enable pin. Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 120 nA, nominal.
GND	B1	3	—	Ground pin.
IN	A2	6	I	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
NC	—	2, 5	—	No connection. This pin can be tied to ground to improve thermal dissipation.
OUT	B2	1	O	Regulated output voltage pin. A small 1-µF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

6 Specifications

6.1 Absolute Maximum Ratings

at T_J = –40°C to +125°C (unless otherwise noted); all voltages are with respect to GND(1)

	MIN	MAX	UNIT
Input voltage range, V_{IN}	–0.3	+6.0	V
Enable voltage range, V_{EN}	–0.3	+6.0(2)	V
Output voltage range, V_{OUT}	–0.3	+6.0	V
Maximum output current, I_{OUT}	Internally limited		
Output short-circuit duration	Indefinite		
Operating junction temperature, T_J	–55	+150	°C
Storage temperature, T_{stg}	–55	+150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} absolute maximum rating is V_{IN} or 6.0 V, whichever is less.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{IN}	Input voltage	2		5.5	V
I_{OUT}	Output current	0		250	mA
T_J	Operating junction temperature range	–40		+125	°C

6.4 Thermal Information

THERMAL METRIC(1)		TPS727		UNITS
		DSE (WSON)	YFF (DSBGA)	
		6 PINS	4 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	190.5	160	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	94.9	75	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	149.3	76	°C/W
ψ_{JT}	Junction-to-top characterization parameter	6.4	3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	152.8	74	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance(2)	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.
(2) θ_{JCbot} is not applicable because there is no thermal pad.

6.5 Electrical Characteristics

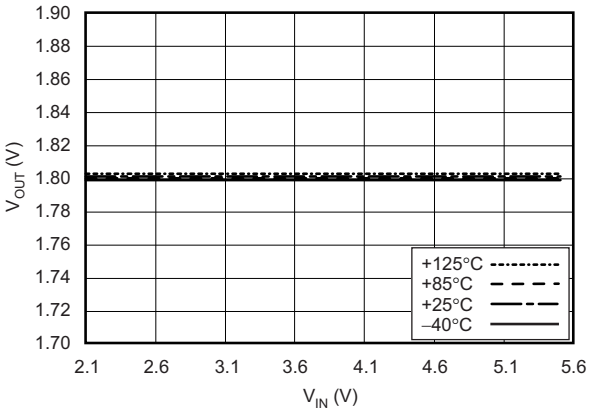
Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = 0.9 V, and C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range			2.0		5.5	V
V_O	Output voltage range			0.9		5.0	V
V_{OUT} (1)	DC output accuracy	T_J = +25°C		–2.5		+2.5	mV
		V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 200 mA		–2.0%	±1.0%	+2.0%	
		V_{OUT} + 0.3 V ≤ V_{IN} ≤ 5.5 V, 0 mA ≤ I_{OUT} ≤ 250 mA			±1.0%		
ΔV_{OUT}	Load transient	1 mA to 200 mA or 200 mA to 1 mA in 1 µs, C_{OUT} = 1 µF			±50.0		mV
		1 mA to 250 mA or 250 mA to 1 mA in 1 µs, C_{OUT} = 1 µF			±65		
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.3 V ≤ V_{IN} ≤ 5.5 V, I_{OUT} = 10 mA			8		µV/V
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0 mA ≤ I_{OUT} ≤ 250 mA			20		µV/mA
V_{DO}	Dropout voltage (2)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 10 mA			6.5		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50 mA			32.5		
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100 mA			65		
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200 mA			130	200	
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 250 mA			162.5		
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$		300	400	550	mA
I_{GND}	Ground pin current	I_{OUT} = 0 mA, T_J = –40°C to +125°C			7.9	12	µA
		I_{OUT} = 200 mA			110		
		I_{OUT} = 250 mA			130		
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4 V, V_{IN} = 2 V, T_J = +25°C			0.12		µA
		V_{EN} ≤ 0.4 V, 2.0 V < V_{IN} ≤ 4.5 V, T_J = –40°C to +85°C			0.55	2	
PSRR	Power-supply rejection ratio	V_{IN} = 2.3 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA	f = 10 Hz		85		dB
			f = 100 Hz		75		
			f = 1 kHz		70		
			f = 10 kHz		55		
			f = 100 kHz		40		
			f = 1 MHz		45		
V_N	Output noise voltage	BW = 100 Hz to 100 kHz, V_{IN} = 2.1 V, V_{OUT} = 1.8 V, I_{OUT} = 10 mA			33.5		μV_{RMS}
t_{STR}	Startup time (3)	C_{OUT} = 1.0 µF, 0 ≤ I_{OUT} ≤ 250 mA			100		µs
V_{HI}	Enable pin high (enabled)			0.9		V_{IN}	V
V_{LO}	Enable pin low (disabled)			0		0.4	V
I_{EN}	Enable pin current	EN = 5.5 V			40	500	nA
UVLO	Undervoltage lock-out	V_{IN} rising		1.85	1.90	1.95	V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing			+160		°C
		Reset, temperature decreasing			+140		
T_J	Operating junction temperature			–40		+125	°C

(1) The output voltage is programmed at the factory.
(2) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35 V so that V_{IN} ≥ 2.3 V.
(3) Startup time: time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

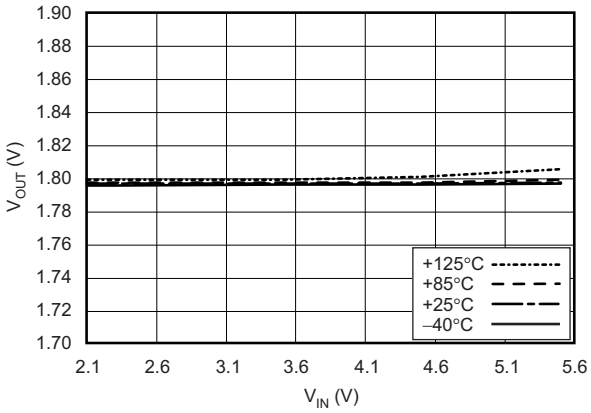
6.6 Typical Characteristics

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J = +25°C.



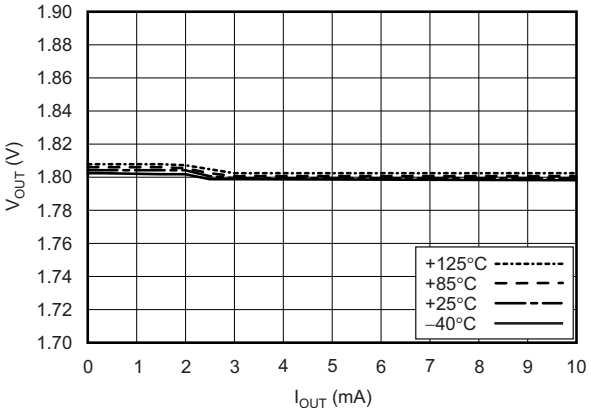
I_{OUT} = 10 mA

Figure 1. Line Regulation (TPS72718)



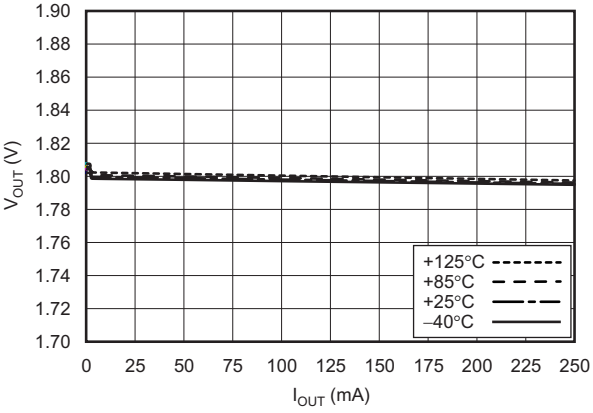
I_{OUT} = 200 mA

Figure 2. Line Regulation (TPS72718)



0 mA ≤ I_{OUT} ≤ 10 mA

Figure 3. Load Regulation Under Light Loads (TPS72718)



0 mA ≤ I_{OUT} ≤ 250 mA

Figure 4. Load Regulation (TPS72718)

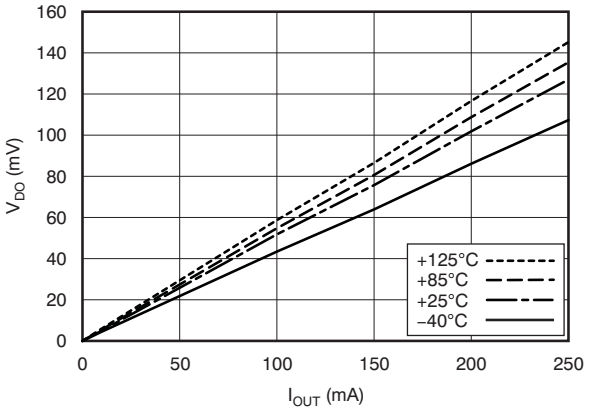
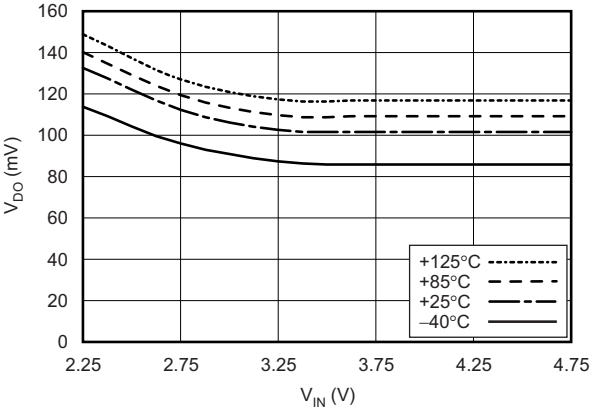


Figure 5. Dropout Voltage vs Output Current (TPS72750)



I_{OUT} = 200 mA

Figure 6. Dropout Voltage vs Input Voltage

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J = +25°C.

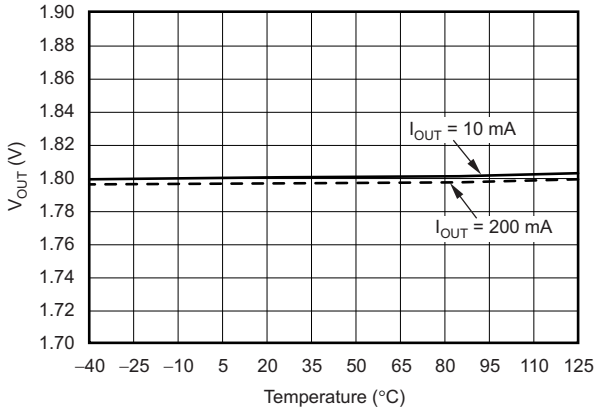
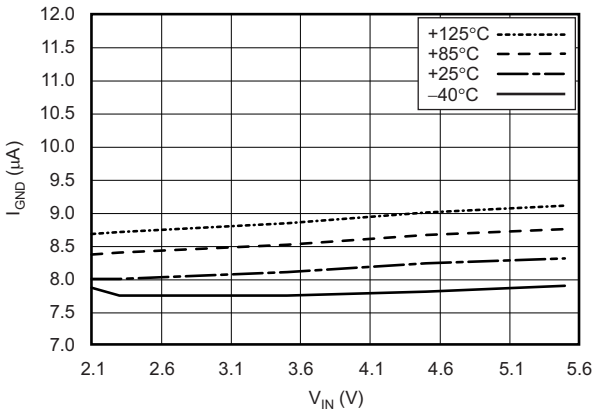
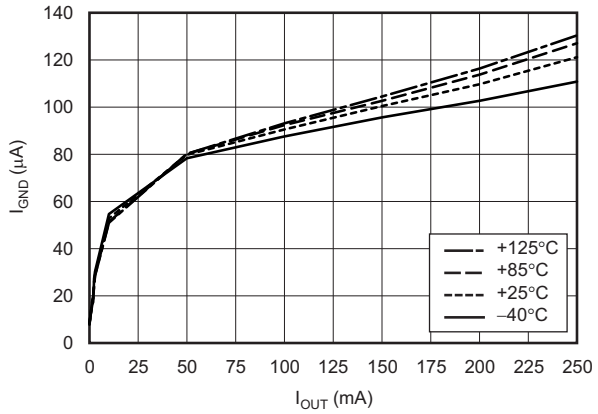


Figure 7. Output Voltage vs Temperature (TPS72718)



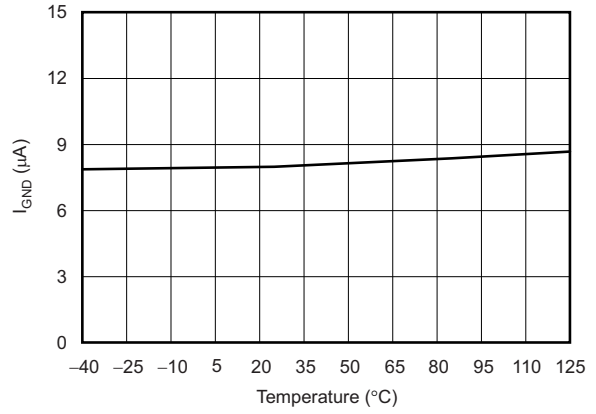
I_{OUT} = 0 mA

Figure 8. Ground Pin Current vs Input Voltage (TPS72718)



0 mA ≤ I_{OUT} ≤ 250 mA

Figure 9. Ground Pin Current vs Load (TPS72718)



V_{IN} = 2.1 V, I_{OUT} = 0 mA

Figure 10. Ground Pin Current vs Temperature (TPS72718)

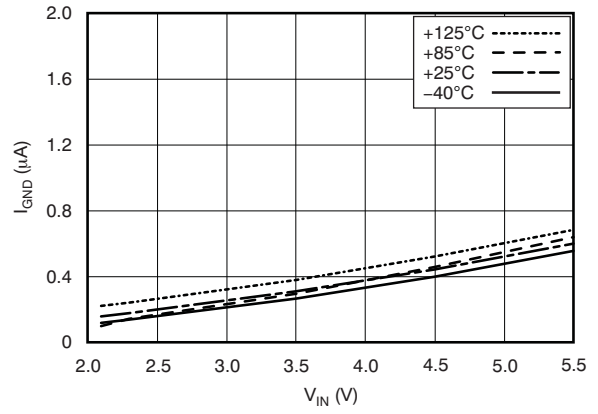


Figure 11. Shutdown Current vs Input Voltage (TPS72718)

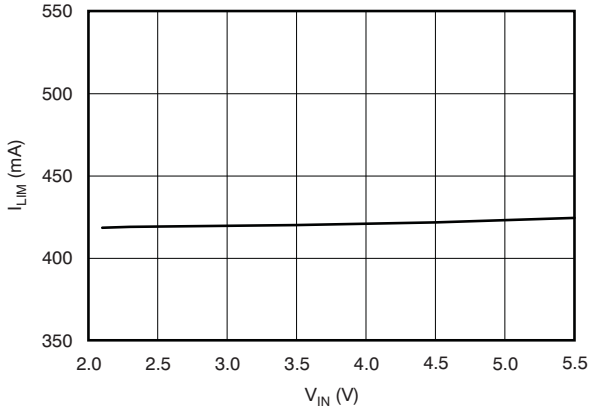


Figure 12. Current Limit vs Input Voltage (TPS72718)

Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J = +25°C.

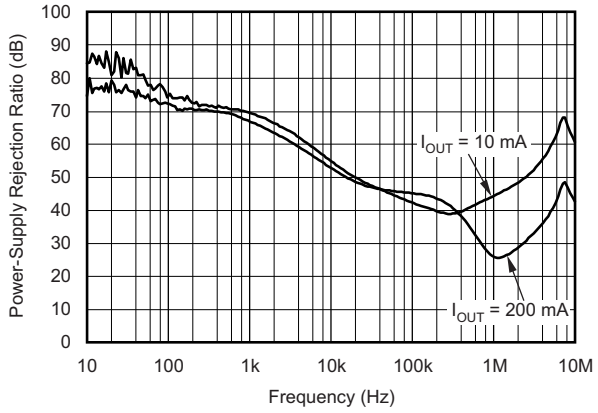


Figure 13. PSRR vs Frequency (V_{IN} – V_{OUT} = 0.5 V, TPS72718)

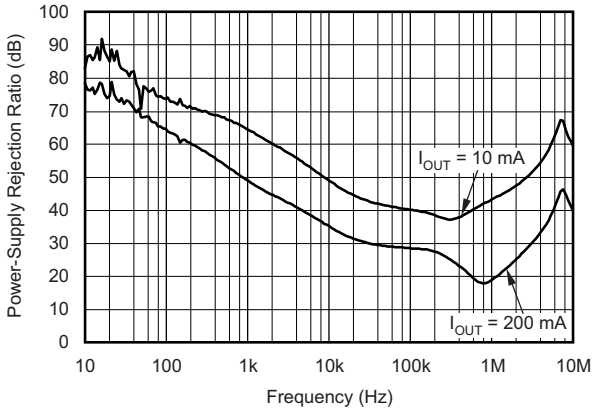


Figure 14. PSRR vs Frequency (V_{IN} – V_{OUT} = 0.3 V, TPS72718)

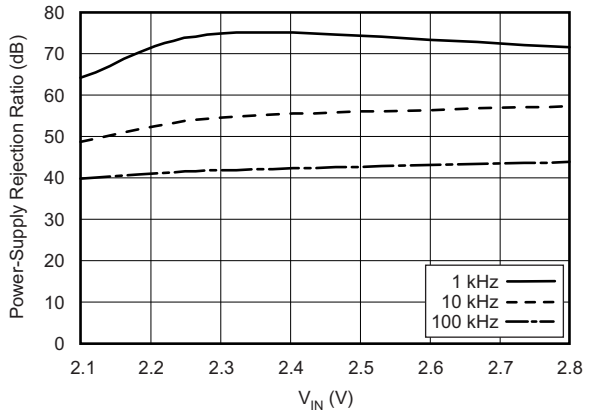
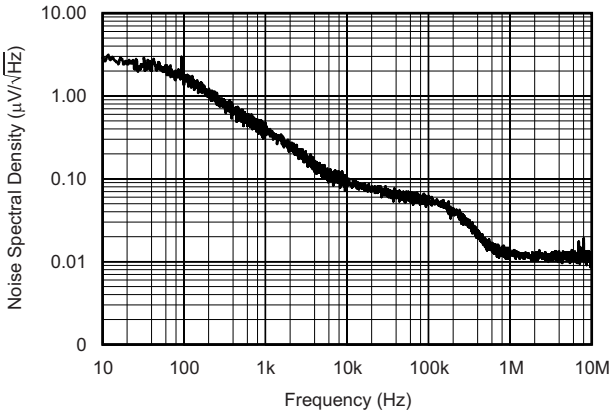
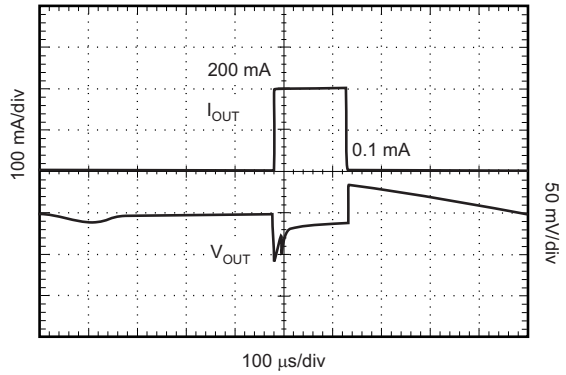


Figure 15. PSRR vs Input Voltage (TPS72718)



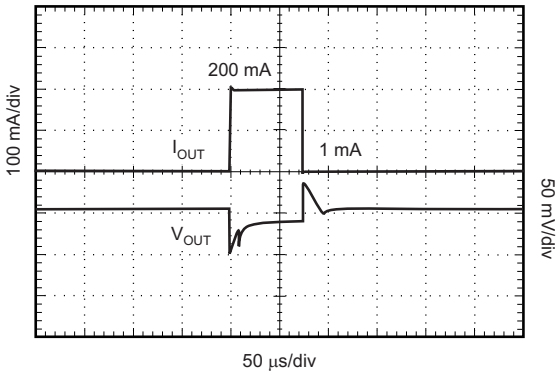
I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF

Figure 16. Output Spectral Noise Density vs Output Voltage (TPS72718)



V_{IN} = 2.3 V, t_R = t_F = 1 µs

Figure 17. Load Transient Response: 0.1 mA to 200 mA (TPS72718)

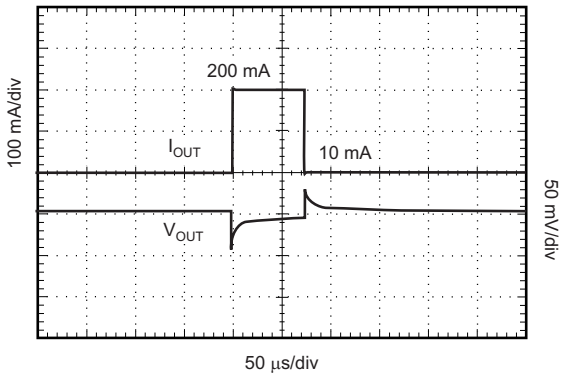


V_{IN} = 2.3 V, t_R = t_F = 1 µs

Figure 18. Load Transient Response: 1 mA to 200 mA (TPS72718)

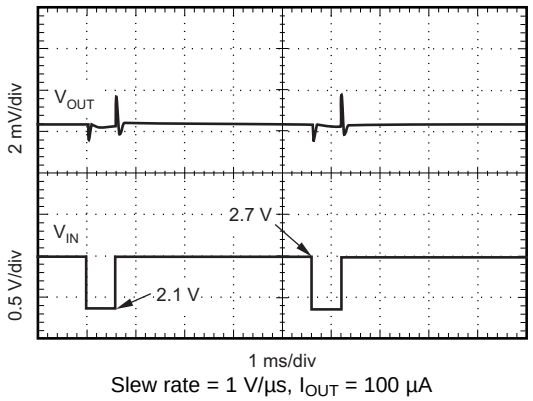
Typical Characteristics (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3 V or 2.0 V, whichever is greater; I_{OUT} = 10 mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0 µF (unless otherwise noted). Typical values are at T_J = +25°C.



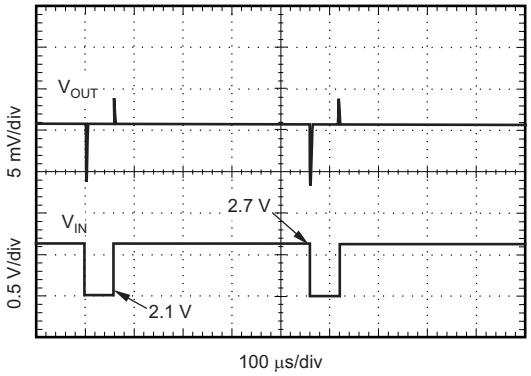
V_{IN} = 2.3 V, t_R = t_F = 1 µs

Figure 19. Load Transient Response: 10 mA to 200 mA (TPS72718)



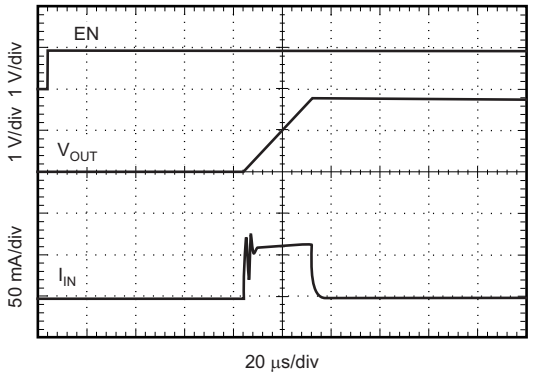
Slew rate = 1 V/µs, I_{OUT} = 100 µA

Figure 20. Line Transient Response (TPS72718)



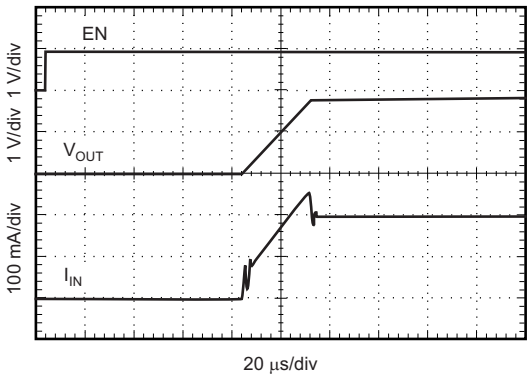
Slew rate = 1 V/µs, I_{OUT} = 200 µA

Figure 21. Line Transient Response (TPS72718)



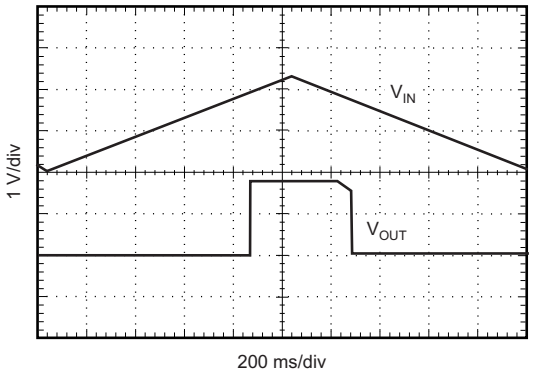
V_{IN} = 2.1 V, V_{OUT} = 1.8 V, I_{OUT} = 100 µA

Figure 22. V_{IN} Inrush Current (TPS72718)



V_{IN} = 2.1 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA

Figure 23. V_{IN} Inrush Current (TPS72718)



I_{OUT} = 200 mA

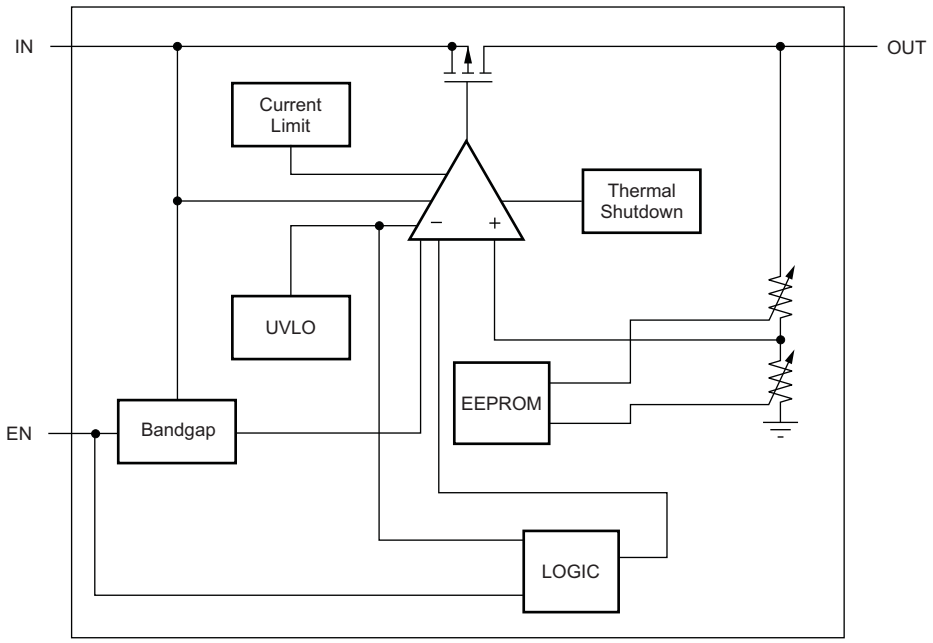
Figure 24. V_{IN} Ramp Up, Ramp Down Response (TPS72718)

7 Detailed Description

7.1 Overview

The TPS727 devices belong to a family of LDO regulators that consume extremely low quiescent current while simultaneously delivering excellent PSRR with very little headroom (V_{IN} – V_{OUT} differential voltage), and very good transient response. These features, combined with low noise without a noise reduction pin in an ultrasmall package, make these devices ideal for portable applications. This family of regulators offers sub-band-gap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The TPS727 internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated and is $V_{OUT} = I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates ($V_{IN} – V_{OUT}$) × I_{LIMIT} until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Protection* section for more details.

The PMOS pass element in the TPS727 has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

7.3.2 Soft Start

The startup current is given by Equation 1:

$$I_{SOFT\ START}\ (mA) = C_{OUT}(\mu F) \times 0.07(V/\mu s) + I_{LOAD}(mA) \quad (1)$$

Equation 1 shows that soft-start current is directly proportional to C_{OUT}.

The output voltage ramp rate is independent of C_{OUT} and load current, and has a typical value of 0.07 V/µs.

Feature Description (continued)

The TPS727 automatically adjusts the soft-start current to supply both the load current and the C_{OUT} charge current. For example, if I_{LOAD} = 0 mA upon enabling the LDO, $I_{SOFT\ START}$ = 1 µF × 0.07 V/µs + 0 mA = 70 mA, the current that charges the output capacitor.

If I_{LOAD} = 200 mA, $I_{SOFT\ START}$ = 1 µF × 0.07 V/µs + 200 mA = 270 mA, the current required for charging output capacitor and supplying the load current.

If the output capacitor and load are increased such that the soft-start current exceeds the output current limit, the current is clamped at the typical current limit of 400 mA. For example, if C_{OUT} = 10 µF and I_{OUT} = 200 mA, 10 µF × 0.07 V/µs + 200 mA = 900 mA is not supplied. Instead, the current is clamped at 400 mA.

7.3.3 Shutdown

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

7.3.4 Dropout Voltage

The TPS727 uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device functions like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is illustrated in Figure 15 in the *Typical Characteristics* section.

7.3.5 Undervoltage Lock-out (UVLO)

The TPS727 uses an undervoltage lock-out circuit that keeps the output shut off until the input voltage reaches the UVLO threshold voltage.

7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, limit junction temperature to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection triggers at least +35°C above the maximum expected ambient condition of a particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS727 is designed to protect against overload conditions. This circuitry is not intended to replace proper heatsinking. Continuously running the TPS727 into thermal shutdown degrades device reliability.

7.4 Device Functional Modes

7.4.1 Operation with EN Control

Driving EN over 0.9 V turns on the regulator. Driving EN below 0.4 V puts the regulator into shutdown mode, thus reducing the operating current to 120 nA, nominal.

8 Applications and Implementation

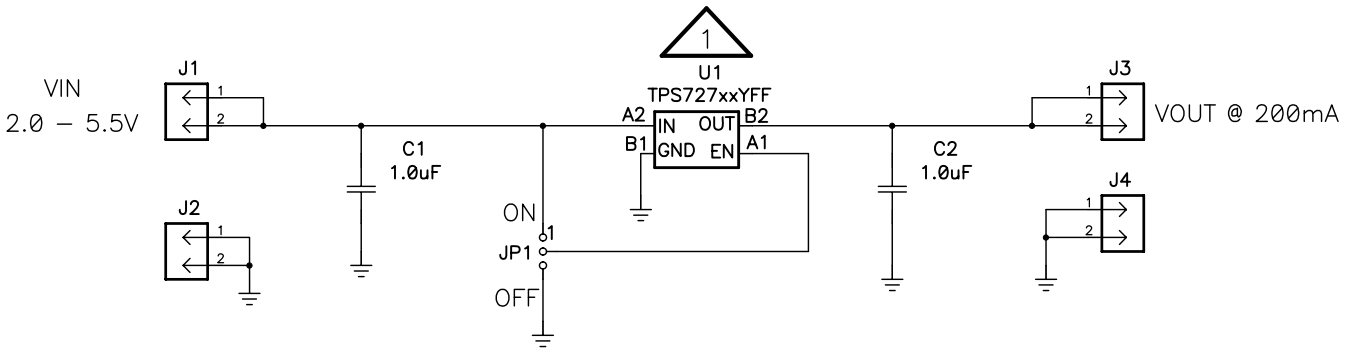
NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS727 family of low-dropout (LDO) linear regulators are utralow quiescent current LDOs with excellent line and ultra-fast load transient performance and are designed for power-sensitive applications.

8.2 Typical Application



1

ASSY	U1	VOUT
–001	TPS72715YFF	1.5V
–002	TPS72718YFF	1.8V
–003	TPS72728YFF	2.8V

Figure 25. TPS72718YFF 2.5 V_{IN} to 1.8 V_{OUT} at 200 mA Schematic

8.2.1 Design Requirements

8.2.1.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, good analog design practice is to connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is not sufficiently low, a 0.1-µF input capacitor may be necessary to ensure stability.

The TPS727 is designed to be stable with standard ceramic capacitors with values of 1.0 µF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR must be less than 200 mΩ.

8.2.1.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces over- and undershoot magnitude but increases duration of the transient response.

Typical Application (continued)

8.2.2 Detailed Design Procedure

Select the desired device based on the output voltage.

Provide an input supply with adequate headroom to include dropout and output current to account for the GND pin current and to power the load.

Select adequate input and output capacitors.

The startup current is given by Equation 2:

$$I_{SOFT\ START}\ (mA) = C_{OUT}(\mu F) \times 0.07(V/\mu s) + I_{LOAD}(mA) \quad (2)$$

Equation 2 shows that soft-start current is directly proportional to C_{OUT}.

The output voltage ramp rate is independent of C_{OUT} and load current and has a typical value of 0.07 V/µs.

The TPS727 automatically adjusts the soft-start current to supply both the load current and the C_{OUT} charge current. For example, if I_{LOAD} = 0 mA upon enabling the LDO, $I_{SOFT\ START}$ = 1 µF × 0.07 V/µs + 0 mA = 70 mA, the current that charges the output capacitor.

If I_{LOAD} = 200 mA, $I_{SOFT\ START}$ = 1 µF × 0.07 V/µs + 200 mA = 270 mA, the current required for charging output capacitor and supplying the load current.

If the output capacitor and load are increased such that the soft-start current exceeds the output current limit, the current is clamped at the typical current limit of 400 mA. For example, if C_{OUT} = 10 µF and I_{OUT} = 200 mA, 10 µF × 0.07 V/µs + 200 mA = 900 mA is not supplied. Instead, the current is clamped at 400 mA.

Typical Application (continued)

8.2.3 Application Curves

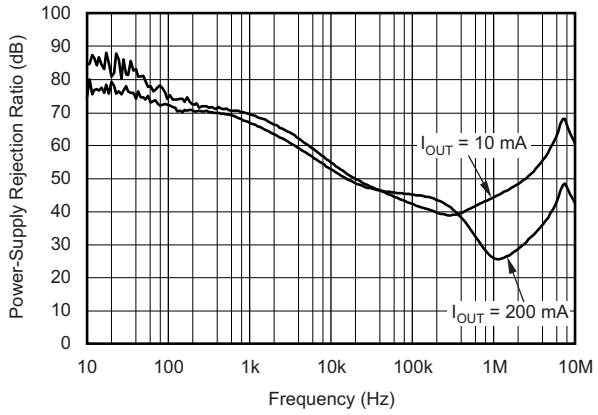
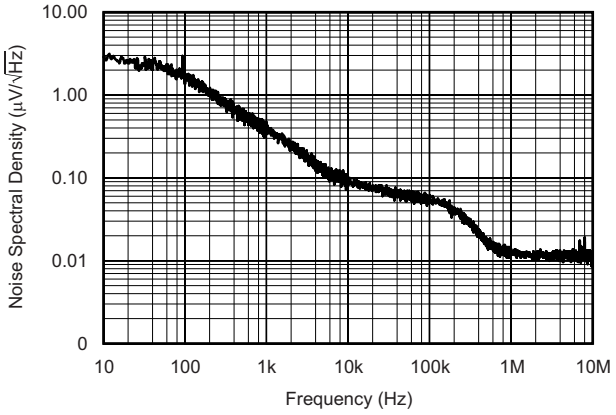
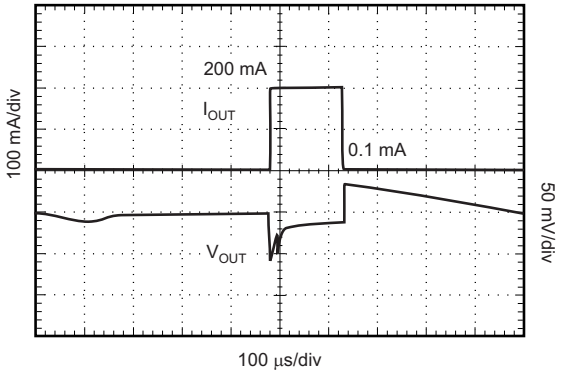


Figure 26. PSRR vs Frequency (V_{IN} – V_{OUT} = 0.5 V, TPS72718)



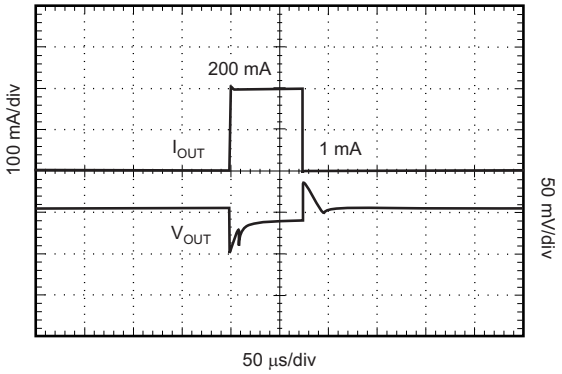
I_{OUT} = 10 mA, C_{IN} = C_{OUT} = 1 µF

Figure 27. Output Spectral Noise Density vs Output Voltage (TPS72718)



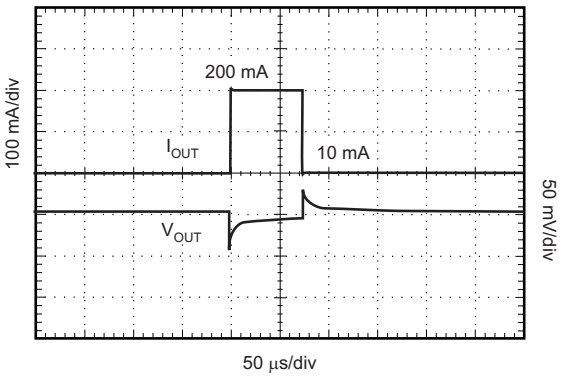
V_{IN} = 2.3 V, t_R = t_F = 1 µs

Figure 28. Load Transient Response: 0.1 mA to 200 mA (TPS72718)



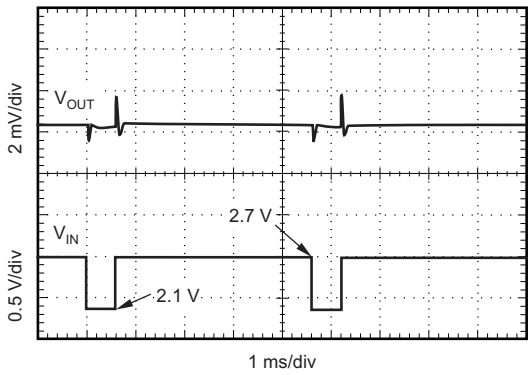
V_{IN} = 2.3 V, t_R = t_F = 1 µs

Figure 29. Load Transient Response: 1 mA to 200 mA (TPS72718)



V_{IN} = 2.3 V, t_R = t_F = 1 µs

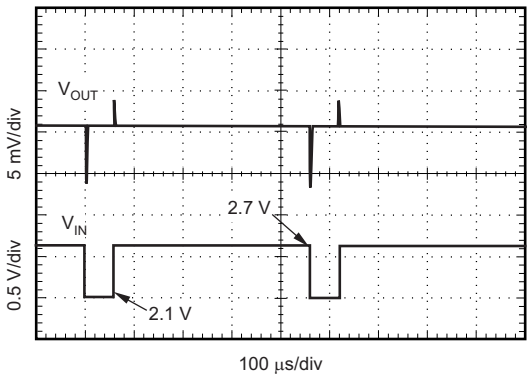
Figure 30. Load Transient Response: 10 mA to 200 mA (TPS72718)



Slew rate = 1 V/µs, I_{OUT} = 100 µA

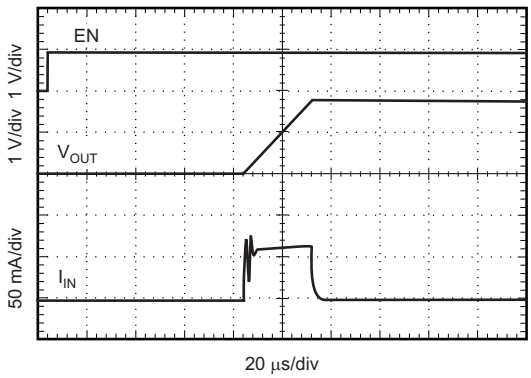
Figure 31. Line Transient Response (TPS72718)

Typical Application (continued)



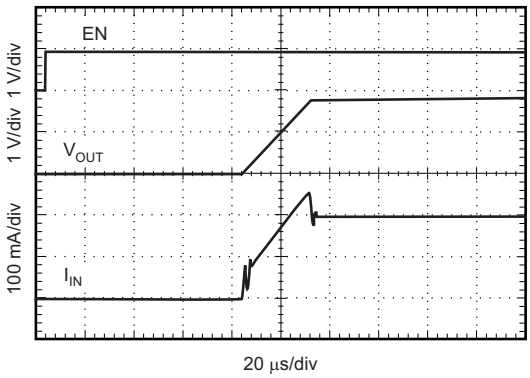
Slew rate = 1 V/µs, I_{OUT} = 200 µA

Figure 32. Line Transient Response (TPS72718)



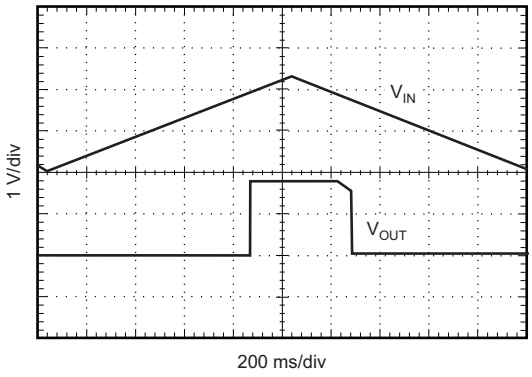
V_{IN} = 2.1 V, V_{OUT} = 1.8 V, I_{OUT} = 100 µA

Figure 33. V_{IN} Inrush Current (TPS72718)



V_{IN} = 2.1 V, V_{OUT} = 1.8 V, I_{OUT} = 200 mA

Figure 34. V_{IN} Inrush Current (TPS72718)



I_{OUT} = 200 mA

Figure 35. V_{IN} Ramp Up, Ramp Down Response (TPS72718)

8.3 Do's and Don'ts

Do place at least one 1.0-µF ceramic capacitor as close as possible to the OUT pin of the regulator.

Do not place the output capacitor more than 10 mm away from the regulator.

For DSE devices, do tie the NC pins to ground to improve thermal dissipation.

Do connect a 0.1-µF to 1.0-µF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator.

Do not exceed the absolute maximum ratings.

9 Power-Supply Recommendations

These devices are designed to operate from an input voltage supply range between 2.0 V and 5.5 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

10 Layout

10.1 Layout Guidelines

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve ac performance (such as PSRR, output noise, and transient response), TI recommends that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor must be connected directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

10.1.2 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Thermal Information* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 3:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (3)$$

10.1.3 Package Mounting

Solder pad footprint recommendations and recommended land patterns are attached to the end of this document.

10.2 Layout Example

10.2.1 DSE EVM Board Layout

This section provides the TPS727xxDSEEVM-406 board layout and illustrations.

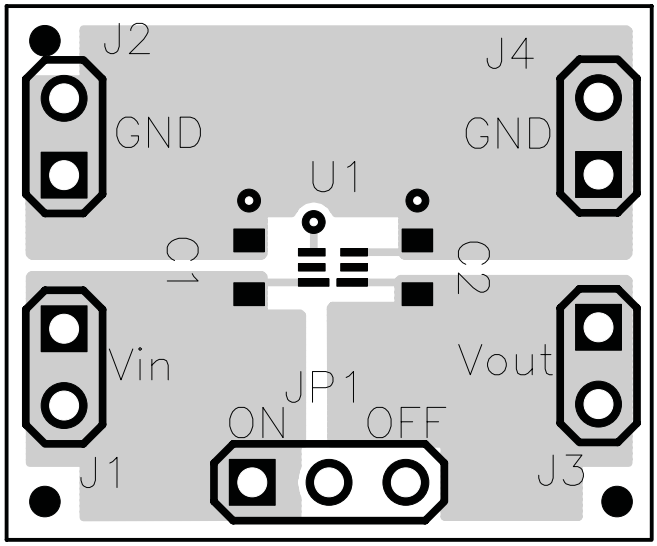


Figure 36. Top Layer Assembly

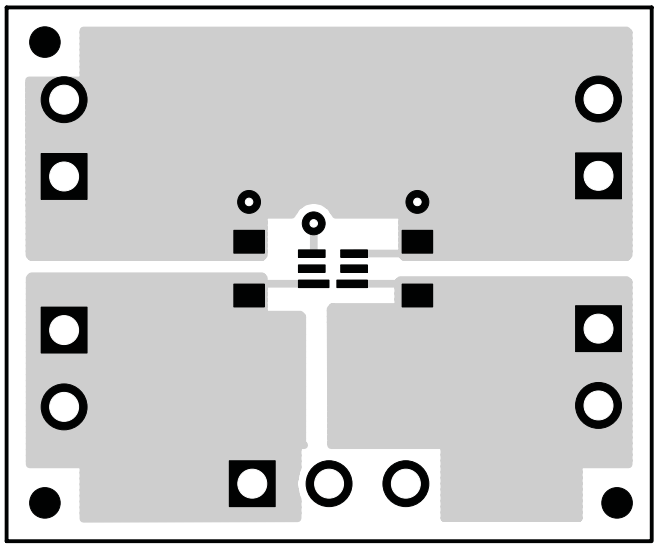


Figure 37. Top Layer Routing

Layout Example (continued)

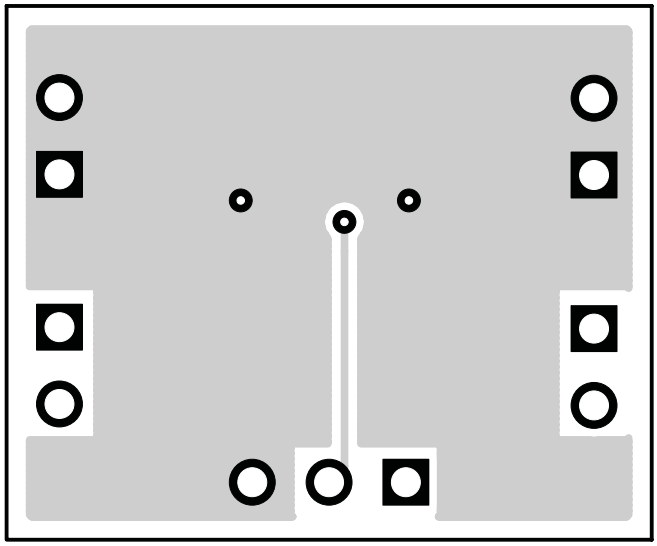


Figure 38. Bottom Layer Routing

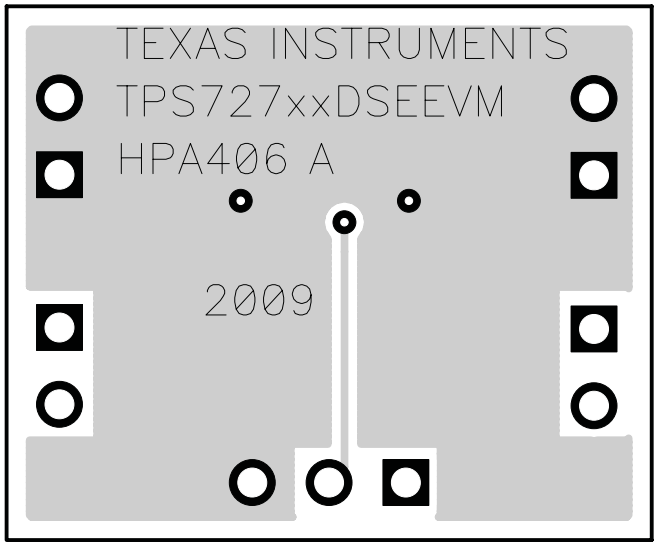


Figure 39. Bottom Layer Assembly

Layout Example (continued)

10.2.2 YFF EVM Board Layout

This section provides the TPS727xxYFFEVM-407 board layout and illustrations.

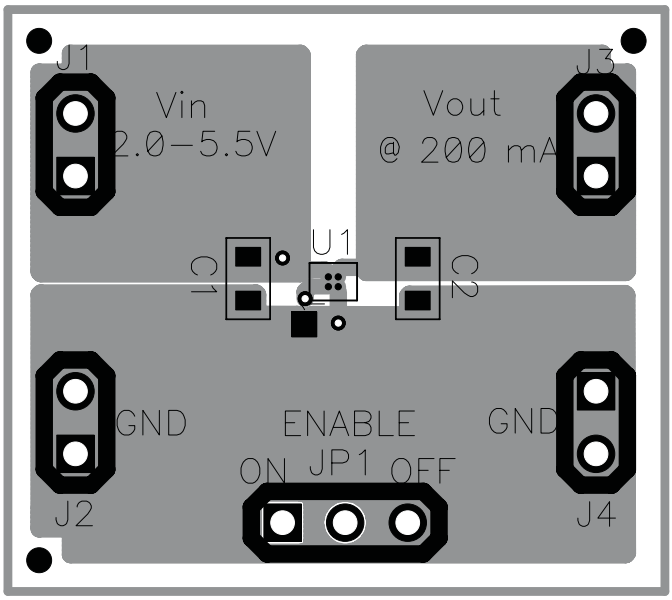


Figure 40. Top Layer Assembly

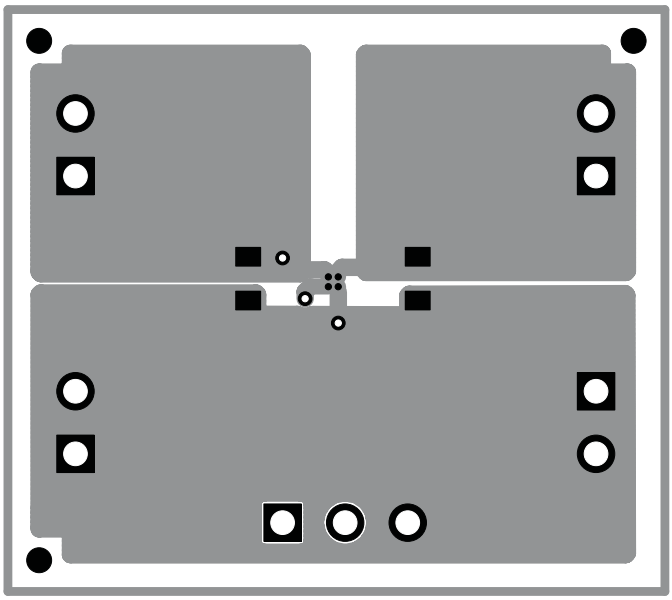


Figure 41. Top Layer Routing

Layout Example (continued)

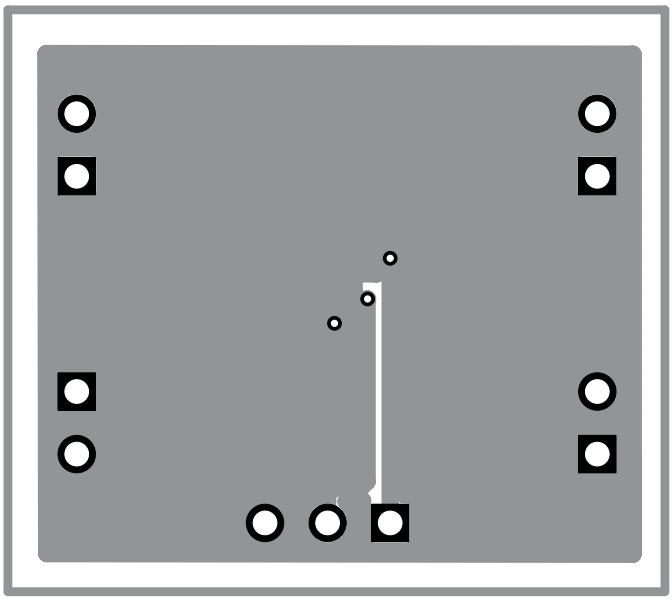


Figure 42. Bottom Layer Routing

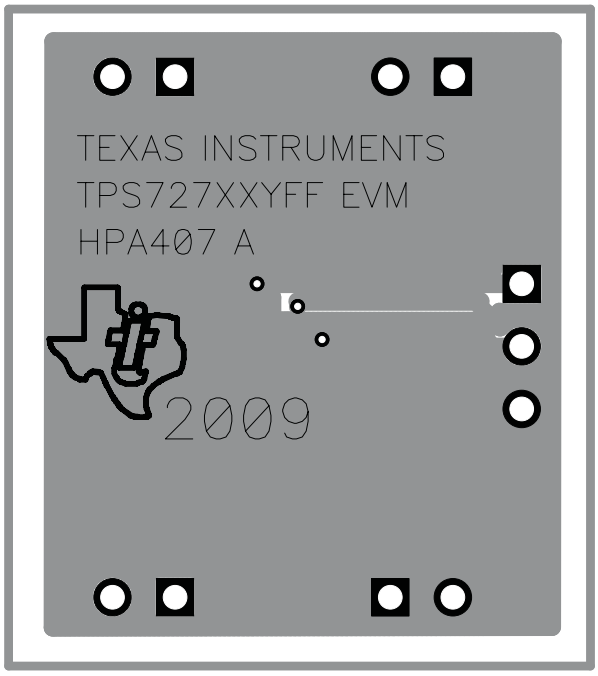


Figure 43. Bottom Layer Assembly

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

Application report SLAA414, *LDO PSRR Measurement Simplified*.

Application report SLAA412, *LDO Noise Demystified*.

User guide SLVU323, *TPS727xxYFF EVM*

User guide SLVU325, *TPS727xxDSE EVM*

11.1.2 Device Nomenclature

Table 1. Device Nomenclature(1)

PRODUCT	V_{OUT} (2)
TPS727**xxx** ***yyy z***	**XXX** is the nominal output voltage. **YYY** is package designator. **Z** is package tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.9 V to 5.0 V in 50-mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG.
Zigbee is a registered trademark of Zigbee Alliance.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.5 Glossary

SLYZ022 — *TI Glossary*.

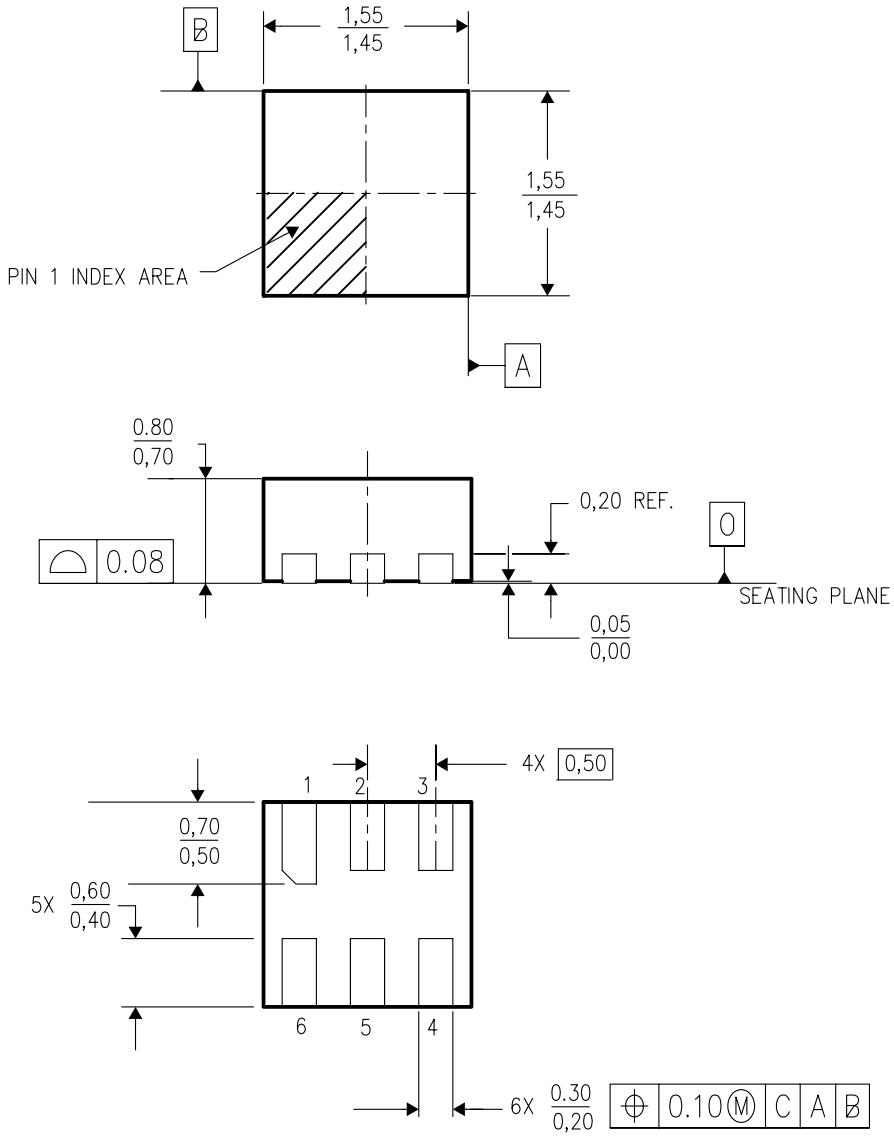
This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

MECHANICAL DATA

DSE (S–PDSO–N6) PLASTIC SMALL OUTLINE

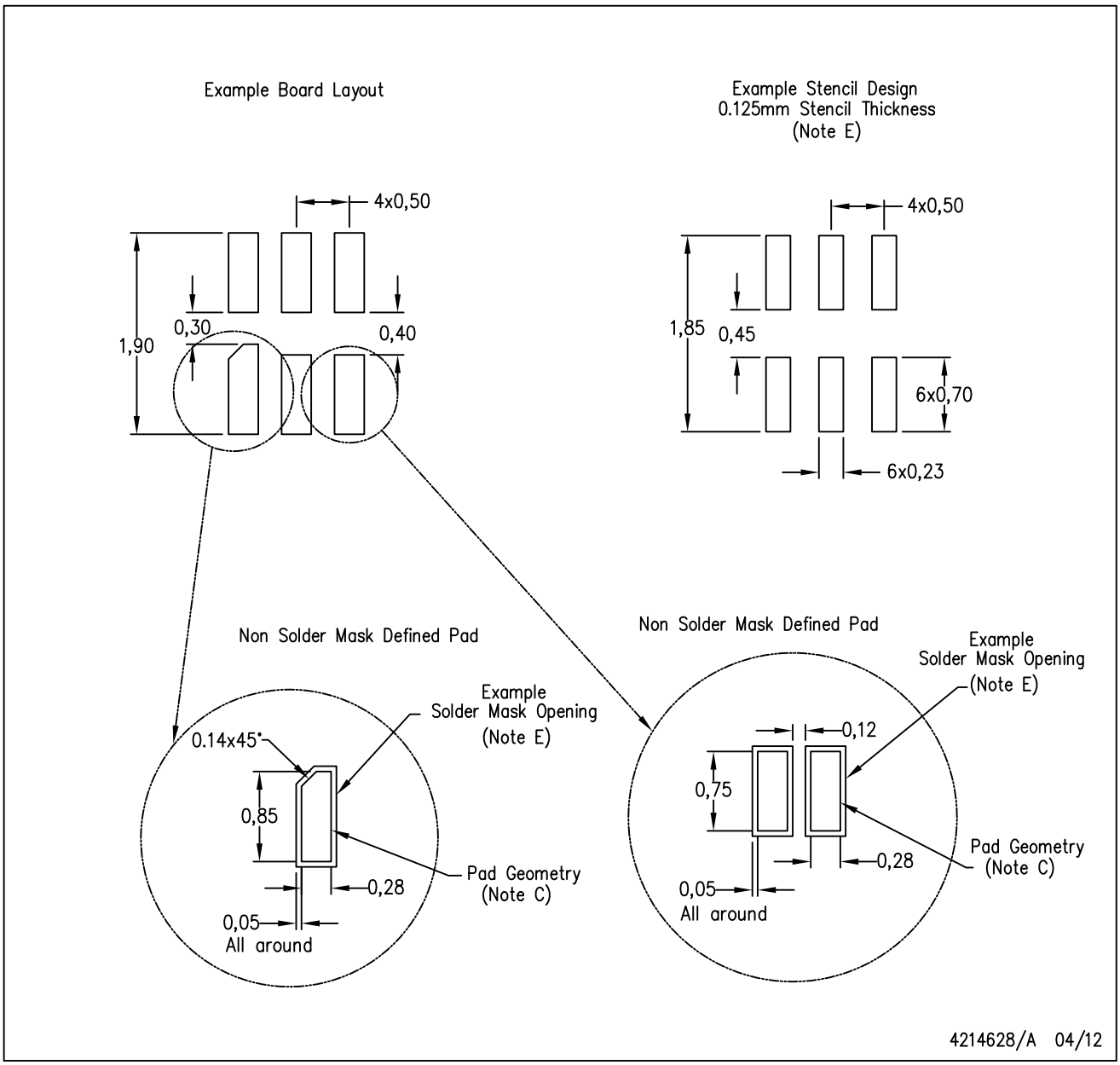


4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. This package is lead–free.

LAND PATTERN DATA

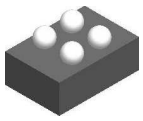
DSE (S–PWSON–N6) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
E. Customers should contact their board fabrication site for solder mask tolerances.

TPS727xxYFF

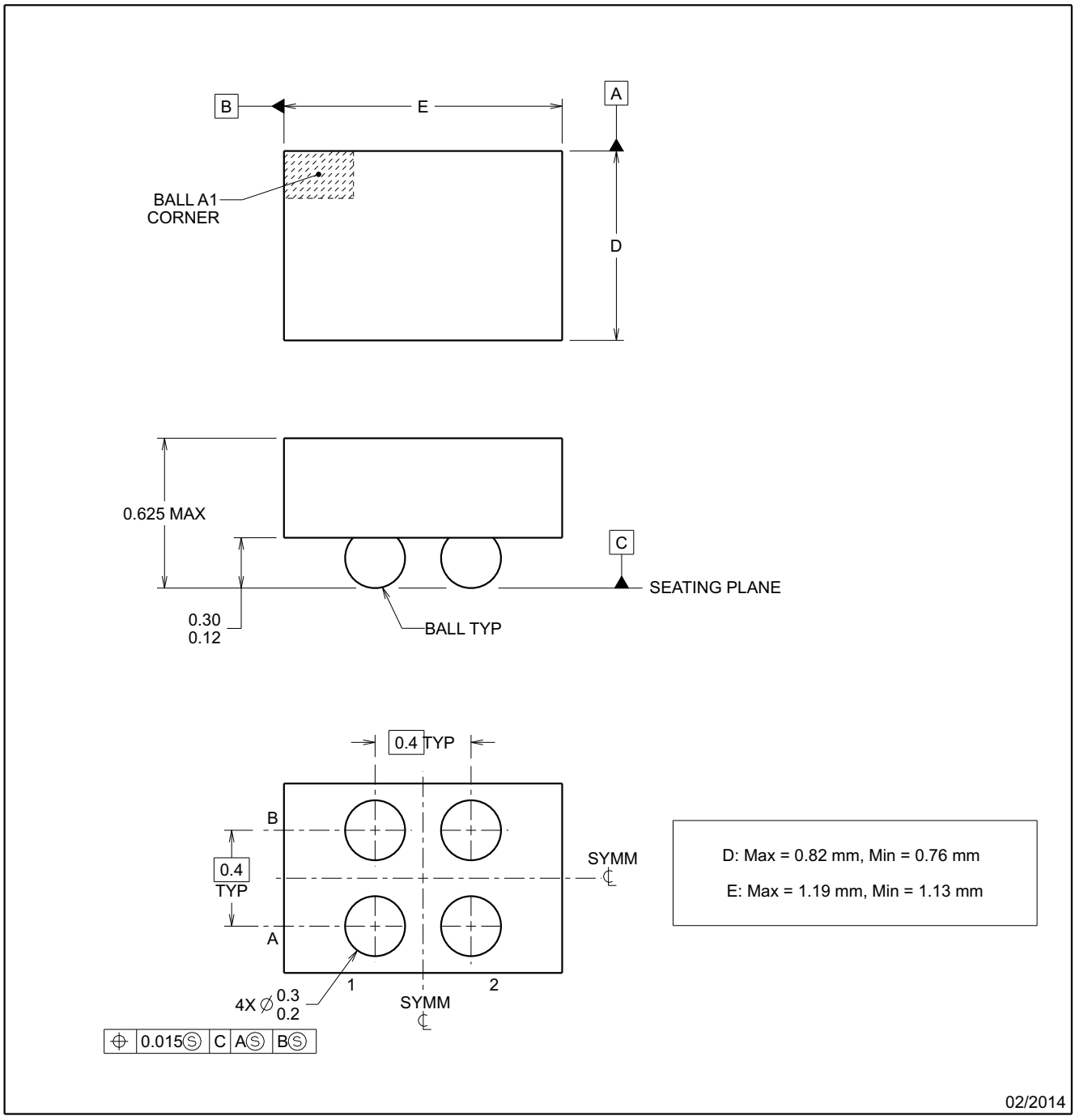
YFF0004



PACKAGE OUTLINE

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. NanoFree™ package configuration.

NanoFree Is a trademark of Texas Instruments.

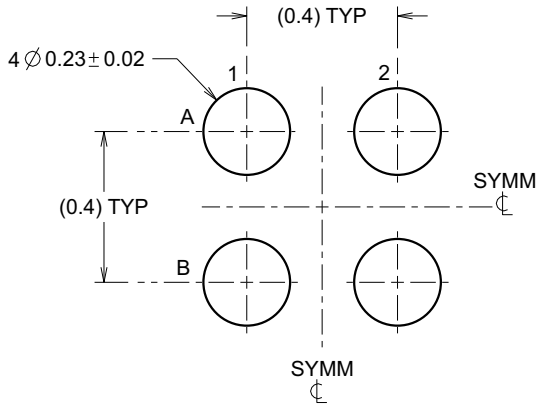
TPS727xxYFF

EXAMPLE BOARD LAYOUT

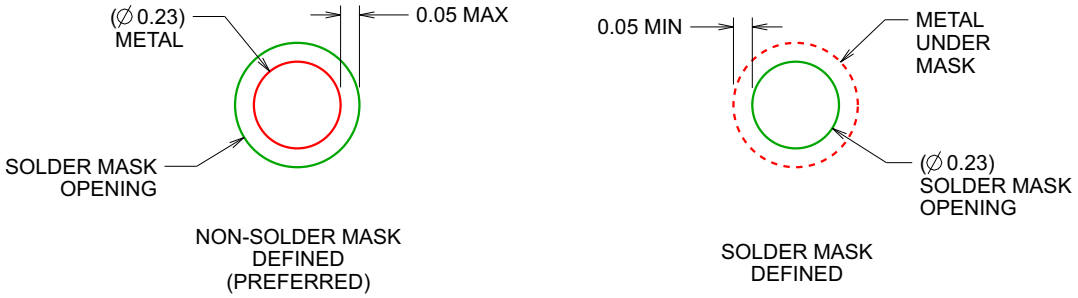
YFF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



LAND PATTERN EXAMPLE
SCALE:50X



SOLDER MASK DETAILS
NOT TO SCALE

02/2014

NOTES: (continued)

4. Final dimensions may vary due to manufacturing tolerance considerations and also routing constraints. Refer to Texas Instruments Literature No. SBVA017 (www.ti.com/lit/sbva017).

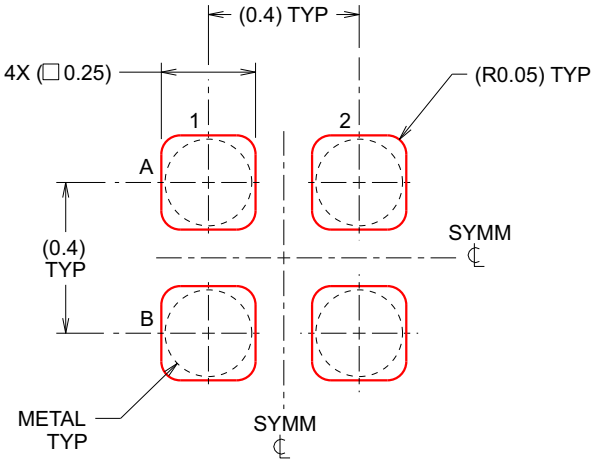
TPS727xxYFF

EXAMPLE STENCIL DESIGN

YFF0004

DSBGA - 0.625 mm max height

DIE SIZE BALL GRID ARRAY



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:50X

02/2014

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS727105YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GA	Samples
TPS727105YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GA	Samples
TPS72710DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UR	Samples
TPS72710DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	UR	Samples
TPS72711YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	QL	Samples
TPS72711YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	QL	Samples
TPS72715DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GS	Samples
TPS72715DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GS	Samples
TPS72715YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GS	Samples
TPS72715YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GS	Samples
TPS727185YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	RW	Samples
TPS727185YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	RW	Samples
TPS72718DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GT	Samples
TPS72718DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GT	Samples
TPS72718YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GT	Samples
TPS72718YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GT	Samples
TPS72719DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CB	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72719DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	CB	Samples
TPS72719YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AA	Samples
TPS72719YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	AA	Samples
TPS72725DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QA	Samples
TPS72725DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QA	Samples
TPS72727DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TS	Samples
TPS72727DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	TS	Samples
TPS727285DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QK	Samples
TPS727285DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QK	Samples
TPS72728DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GU	Samples
TPS72728DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	GU	Samples
TPS72728YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
TPS72728YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	GU	Samples
TPS72730DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QB	Samples
TPS72730DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QB	Samples
TPS72730YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZZ	Samples
TPS72730YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZZ	Samples
TPS72733DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QC	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS72733DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM	-40 to 125	QC	Samples
TPS72733YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZY	Samples
TPS72733YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	ZY	Samples
TPS72748YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EY	Samples
TPS72748YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	EY	Samples
TPS72750YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CA	Samples
TPS72750YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-40 to 125	CA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

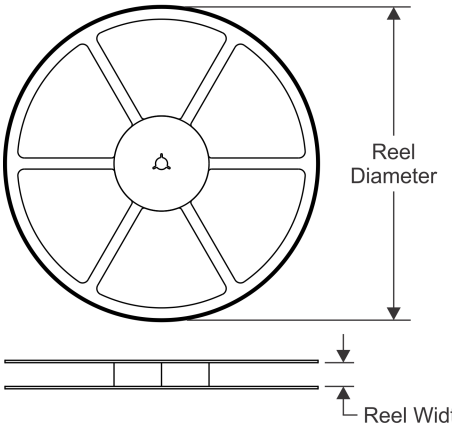
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

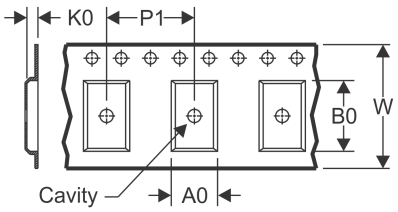
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

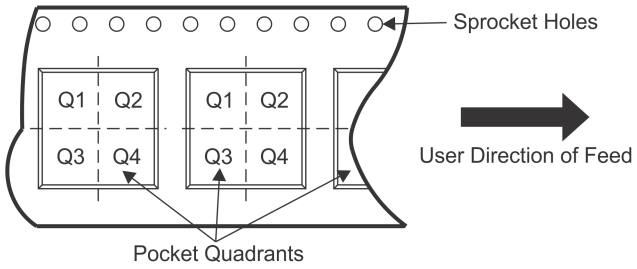


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

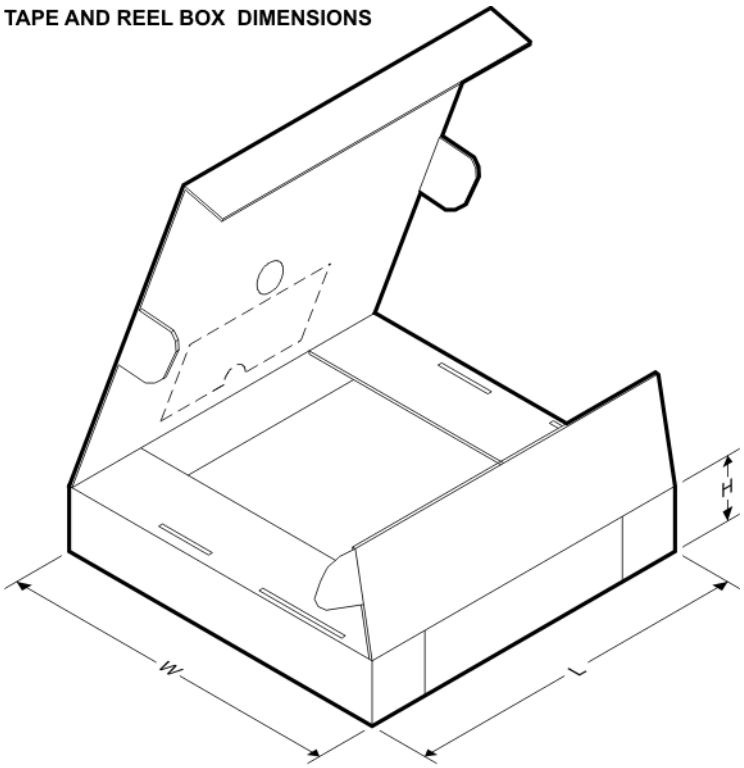


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS727105YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS727105YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72710DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72710DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72710DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72710DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72711YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72711YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72715DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72715DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72715YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72715YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS727185YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS727185YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72718DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72718DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72718YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72718YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS72719DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72719DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72719DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72719DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72719YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72719YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72725DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72725DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72727DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72727DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72727DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72727DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS727285DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS727285DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS727285DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS727285DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72728DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72728DSER	WSON	DSE	6	3000	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72728DSET	WSON	DSE	6	250	179.0	8.4	1.8	1.8	1.0	4.0	8.0	Q2
TPS72728DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72728YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72728YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72730DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72730DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72730YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72730YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72733DSER	WSON	DSE	6	3000	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72733DSET	WSON	DSE	6	250	178.0	8.4	1.7	1.7	0.95	4.0	8.0	Q2
TPS72733YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72733YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72748YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72748YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q2
TPS72750YFFR	DSBGA	YFF	4	3000	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1
TPS72750YFFT	DSBGA	YFF	4	250	180.0	8.4	0.89	1.26	0.69	4.0	8.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS727105YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS727105YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72710DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72710DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72710DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72710DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72711YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72711YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72715DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72715DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72715YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72715YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS727185YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS727185YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72718DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72718DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72718YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72718YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72719DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72719DSER	WSON	DSE	6	3000	203.0	203.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS72719DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72719DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72719YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72719YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72725DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72725DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72727DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72727DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72727DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72727DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS727285DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS727285DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS727285DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS727285DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72728DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72728DSER	WSON	DSE	6	3000	203.0	203.0	35.0
TPS72728DSET	WSON	DSE	6	250	203.0	203.0	35.0
TPS72728DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72728YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72728YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72730DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72730DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72730YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72730YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72733DSER	WSON	DSE	6	3000	205.0	200.0	33.0
TPS72733DSET	WSON	DSE	6	250	205.0	200.0	33.0
TPS72733YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72733YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72748YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72748YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0
TPS72750YFFR	DSBGA	YFF	4	3000	182.0	182.0	20.0
TPS72750YFFT	DSBGA	YFF	4	250	182.0	182.0	20.0

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