SLUS247F − APRIL 1997 − REVISED NOVEMBER 2007

MICROPROCESSOR SUPERVISOR WITH WATCHDOG TIMER

FEATURES

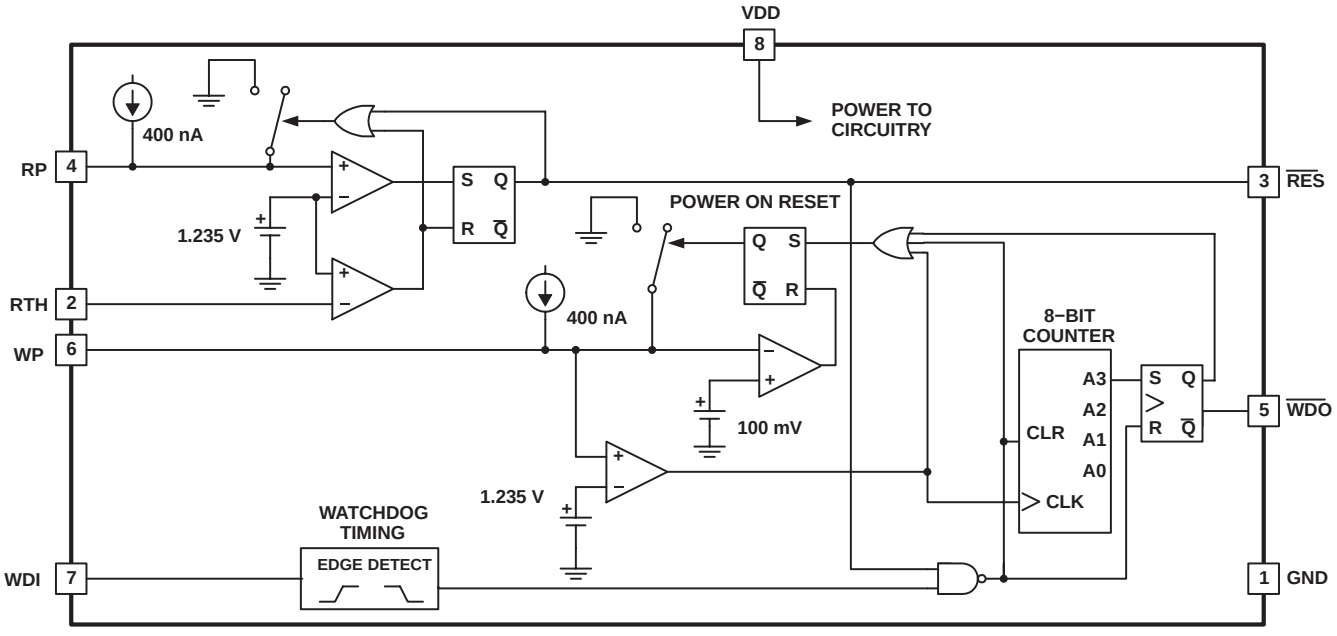
- **Fully Programmable Reset Threshold**
- **Fully Programmable Reset Period**
- **Fully Programmable Watchdog Period**
- **2% Accurate Reset Threshold**
- **Input Voltage Down to 2 V**
- **Input 18-μA Maximum Input Current**
- **Reset Valid Down to 1 V**

DESCRIPTION

The UCCx946 is designed to provide accurate microprocessor supervision, including reset and watchdog functions. During power up, the device asserts a reset signal $\overline{RES}$ with VDD as low as 1 V. The reset signal remains asserted until the VDD voltage rises and remains above the reset threshold for the reset period. Both reset threshold and reset period are programmable by the user.

The UCCx946 is also resistant to glitches on the VDD line. Once $\overline{RES}$ has been deasserted, any drops below the threshold voltage need to be of certain time duration and voltage magnitude to generate a reset signal. These values are shown in Figure 1. An I/O line of the microprocessor may be tied to the watchdog input (WDI) for watchdog functions. If the I/O line is not toggled within a set watchdog period, programmable by the user, WDO is asserted. The watchdog function is disabled during reset conditions.

The UCCx946 is available in 8-pin SOIC(D), 8-pin PDIP (N) and 8-pin TSSOP(PW) packages to optimize board space.



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ORDERING INFORMATION

T_A	PACKAGED DEVICES(3)		
	(D)	(N)	(PW)
−40°C to 95°C	UCC2946D	UCC2946N	UCC2946PW
0°C to 70°C	UCC3946D	UCC3946N	UCC3946PW

(1) The D and PW packages are also available taped and reeled. Add an R suffix to the device type (i.e., UCC2946DR) for quantities of 3,000 devices per reel.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

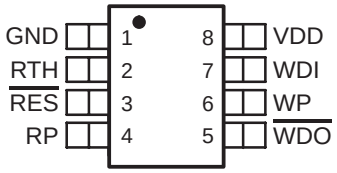
ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UCC2946 UCC3946	UNIT
Input voltage range, V_{IN}	10	V
Junction temperature range, T_J	−55 to 150	°C
Storage temperature, T_{stg}	−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. Voltages are with respect to GND. Currents are positive into, and negative out of the specified terminal.

D PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
GND	1	−	Ground reference for the device
$\overline{\text{RES}}$	3	O	This pin is high only if the voltage on the RTH has risen above 1.235 V. Once RTH rises above the threshold, this pin remains low for the reset period. This pin asserts low and remains low if the RTH voltage dips below 1.235 V for an amount of time determined by Figure 1.
RTH	2	I	This input compares its voltage to an internal 1.25-V reference. By using external resistors, a user can program any desired reset threshold.
RP	4	I	This pin allows the user to program the reset period by adjusting an external capacitor.
VDD	8	I	Supply voltage for the device.
WDI	7	I	This pin is the input to the watchdog timer. If this pin is not toggled or strobed within the watchdog period, $\overline{\text{WDO}}$ is asserted.
$\overline{\text{WDO}}$	5	O	This pin is the watchdog output. This pin is asserted low if the WDI pin is not strobed or toggled within the watchdog period.
WP	6	I	This pin allows the user to program the watchdog period by adjusting an external capacitor.

ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C and 2.0 V ≤ V_{DD} ≤ 5.5 V for the UCC3946, T_A = −40°C to 95°C and 2.1 V ≤ V_{DD} ≤ 5.5 V for the UCC2946, (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
REFERENCE							
V_{DD}	Operating voltage	UCC2946		2.1		5.5	V
		UCC3946		2.0		5.5	
I_{DD}	Supply current	UCC2946			12	18	µA
		UCC3946			10	18	
$V_{DD(min)}$	Minimum operating voltage(1)	UCC2946				1.1	V
		UCC3946				1.0	
RESET SECTION							
	Reset threshold voltage	UCC2946	V_{DD} rising	1.170	1.235	1.260	V
		UCC3946		1.190	1.235	1.260	
	Threshold hysteresis				15		mV
I_{LEAK}	Input leakage current					5	nA
V_{OH}	High-level output voltage		I_{SOURCE} = 2 mA	V_{DD}–0.3			V
V_{OL}	Low-level output voltage		I_{SINK} = 2 mA			0.1	
		UCC2946	I_{SINK} = 20 µA, VDD = 1 V			0.4	
		UCC3946				0.2	
	VDD-to-output delay time		VDD = −1 mV/µs		120		µs
	Reset period	UCC2946	C_{RP} = 64 nF	140	200	320	ms
		UCC3946		160	200	260	
WATCHDOG SECTION							
V_{IH}	High-level input voltage, WDI			0.7×V_{DD}			V
V_{IL}	Low-level input voltage, WDI					0.3×V_{DD}	
	Watchdog period	UCC2946	C_{RP} = 64 nF	0.96	1.60	2.56	s
		UCC3946		1.12	1.60	2.08	
	Watchdog pulse width			50			ns
V_{OH}	High-level output voltage		I_{SOURCE} = 2 mA	V_{DD}–0.3			V
V_{OL}	Low-level output voltage		I_{SINK} = 2 mA			0.1	

(1) Minimum supply voltage where $\overline{RES}$ is considered valid.

APPLICATION INFORMATION

The UCCx946 supervisory circuit provides accurate reset and watchdog functions for a variety of microprocessor applications. The reset circuit prevents the microprocessor from executing code during undervoltage conditions, typically during power-up and power-down. In order to prevent erratic operation in the presence of noise, voltage glitches where voltage amplitude and time duration are less than the values specified in Figure 1 are ignored.

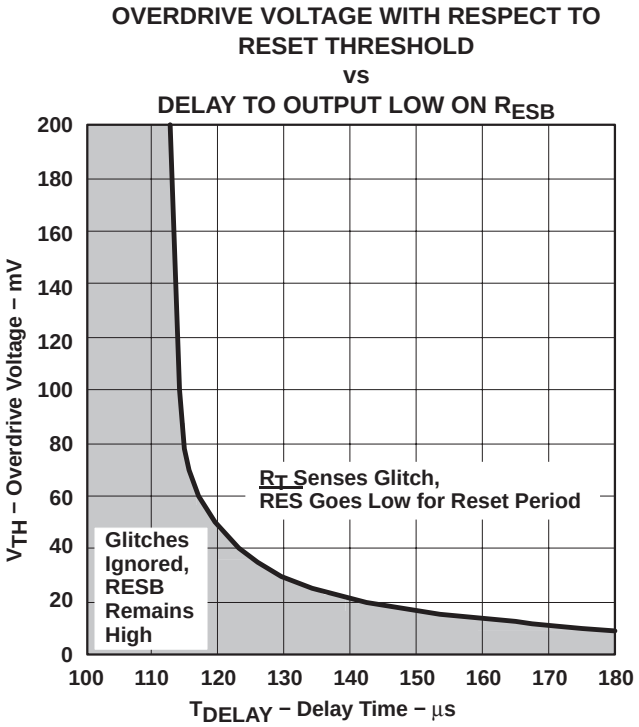


Figure 1.

The watchdog circuit monitors the microprocessor's activity, if the microprocessor does not toggle WDI during the programmable watchdog period $\overline{WDO}$ goes low, alerting the microprocessor's interrupt of a fault. The $\overline{WDO}$ pin is typically connected to the non-maskable input of the microprocessor so that an error recovery routine can be executed.

APPLICATION INFORMATION

PROGRAMMING THE RESET VOLTAGE AND RESET PERIOD

The UCCx946 allows the reset trip voltage to be programmed with two external resistors. In most applications VDD is monitored by the reset circuit, however, the design allows voltages other than VDD to be monitored. Referring to Figure 2, the voltage below which reset is asserted is determined by:

$$V_{RESET} = 1.235 \times \left(\frac{R1 + R2}{R2}\right) \quad (1)$$

In order to keep quiescent currents low, resistor values in the megaohm range can be used for R1 and R2. A manual reset can be easily implemented by connecting a momentary push switch in parallel with R2. $\overline{RES}$ is ensured to be low with VDD voltages as low as 1 V.

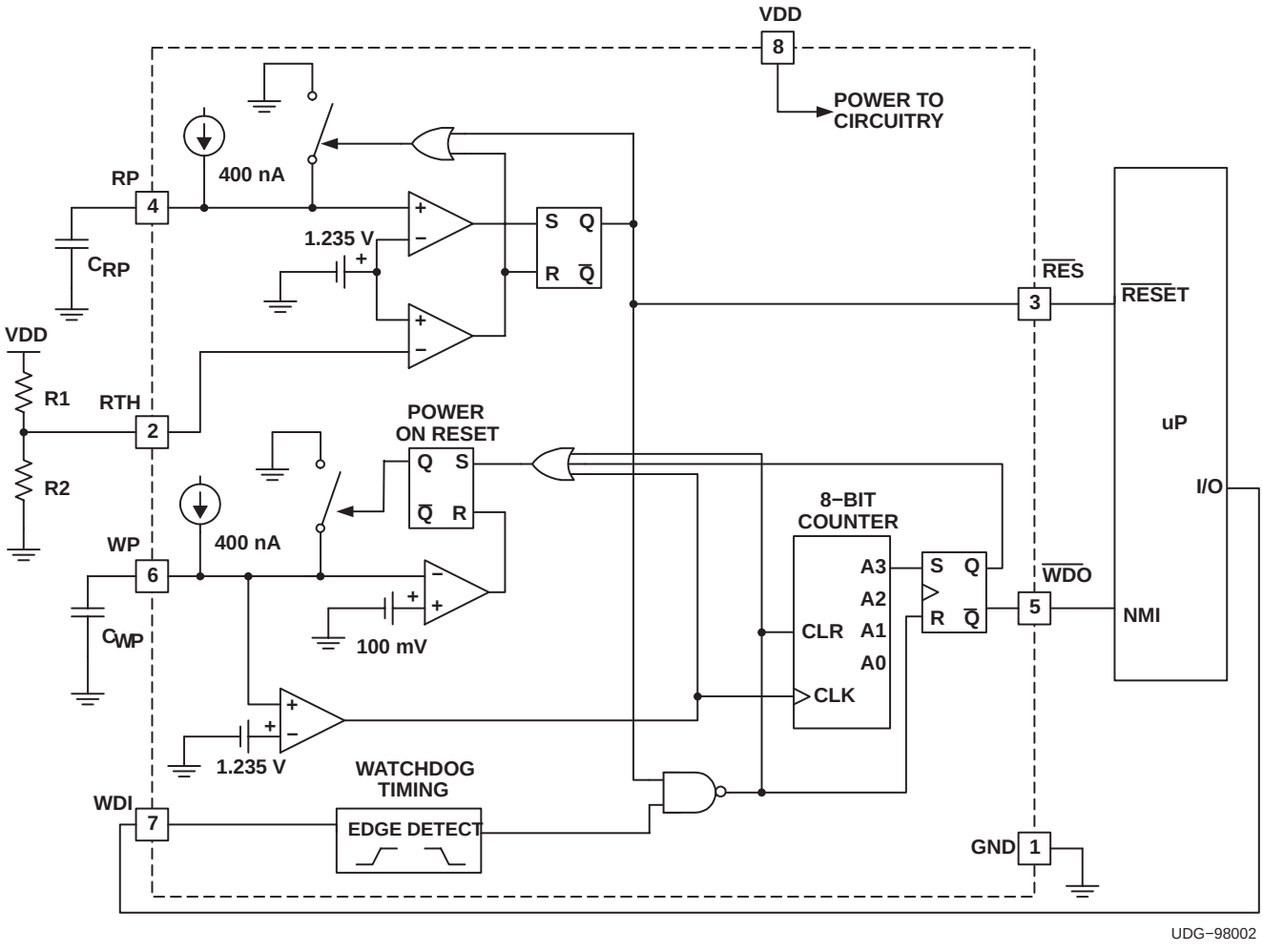


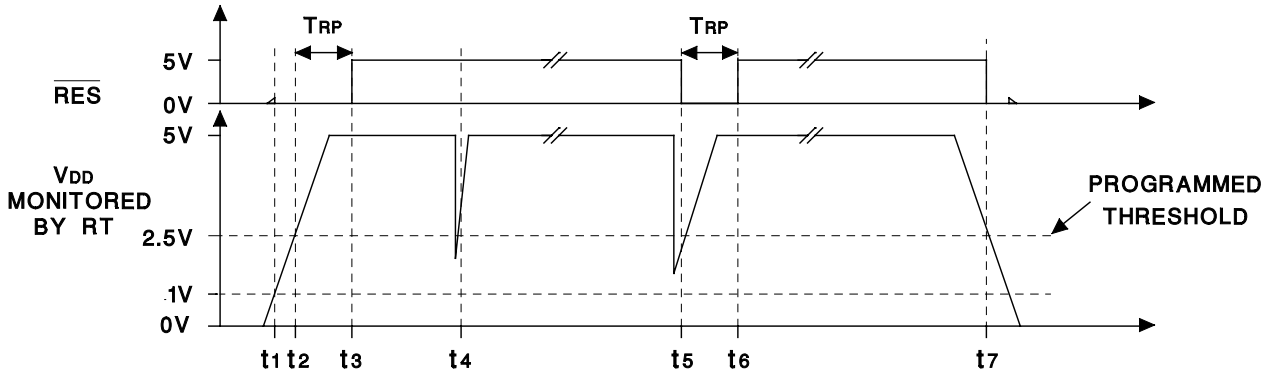
Figure 2. Typical Application Diagram

APPLICATION INFORMATION

Once VDD rises above the programmed threshold, $\overline{RES}$ remains low for the reset period defined by:

$$T_{RP} = 3.125 \times C_{RP} \quad (2)$$

where T_{RP} is time in milliseconds and C_{RP} is capacitance in nanofarads. C_{RP} is charged with a precision current source of 400 nA, a high-quality, low-leakage capacitor (such as an NPO ceramic) should be used to maintain timing tolerances. Figure 3 illustrates the voltage levels and timings associated with the reset circuit.



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t1: VDD > 1 V, $\overline{RES}$ is ensured low.
t2: VDD > programmed threshold, $\overline{RES}$ remains low for TRP.
t3: T_{RP} expires, $\overline{RES}$ pulls high.
t4: Voltage glitch occurs, but is filtered at the RTH pin, $\overline{RES}$ remains high.
t5: Voltage glitch occurs whose magnitude and duration is greater than the RTH filter, $\overline{RES}$ is asserted for TRP.
t6: On completion of the TRP pulse the RTH voltage has returned and $\overline{RES}$ is pulled high.
t7: VDD dips below threshold (minus hysteresis), $\overline{RES}$ is asserted.

Figure 3. Reset Circuit Timings

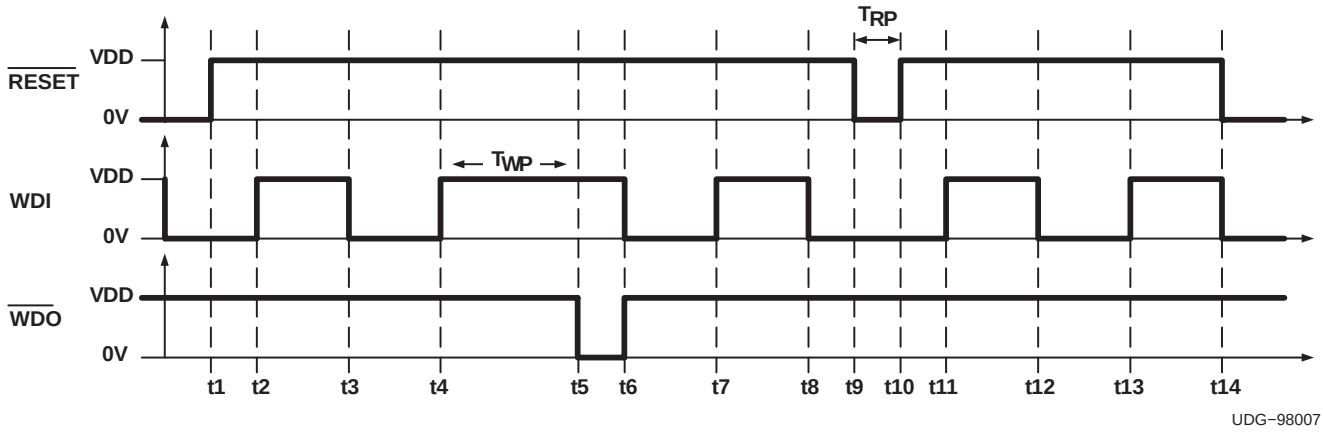
APPLICATION INFORMATION

PROGRAMMING THE WATCHDOG PERIOD

The watchdog period is programmed with C_{WP} as follows:

$$T_{WP} = 25 \times C_{WP} \quad (3)$$

where T_{WP} is in milliseconds and C_{WP} is in nanofarads. A high-quality, low-leakage capacitor should be used for C_{WP}. The watchdog input WDI must be toggled with a high-to-low or low-to-high transition within the watchdog period to prevent $\overline{WDO}$ from assuming a logic level low. $\overline{WDO}$ maintains the low logic level until WDI is toggled or $\overline{RES}$ is asserted. If at any time $\overline{RES}$ is asserted, $\overline{WDO}$ assumes a high logic state and the watchdog period be reinitiated. Figure 4 illustrates the timings associated with the watchdog circuit.



t1: Microprocessor is reset.
t2: WDI is toggled some time after reset, but before TWP expires.
t3: WDI is toggled before T_{WP} expires.
t4: WDI is toggled before T_{WP} expires.
t5: WDI is not toggled before TWP expires and $\overline{WDO}$ asserts low, triggering the microprocessor to enter an error recovery routine.
t6: The microprocessor's error recovery routine is executed and WDI is toggled, reinitiating the watchdog timer.
t7: WDI is toggled before T_{WP} expires.
t8: WDI is toggled before T_{WP} expires.
t9: $\overline{RES}$ is momentarily triggered, $\overline{RES}$ is asserted low for $\overline{TRP}$.
t10: Microprocessor is reset, $\overline{RES}$ pulls high.
t11: WDI is toggled some time after reset, but before T_{WP} expires.
t12: WDI is toggled before T_{WP} expires.
t13: WDI is toggled before T_{WP} expires.
t14: VDD dips below the reset threshold, $\overline{RES}$ is asserted.

Figure 4. Watchdog Circuit Timings

APPLICATION INFORMATION

CONNECTING $\overline{\text{WDO}}$ TO $\overline{\text{RES}}$

In order to provide design flexibility, the reset and watchdog circuits in the UCCx946 have separate outputs. Each output independently drives high or low, depending on circuit conditions explained previously.

In some applications, it may be desirable for either the $\overline{\text{RES}}$ or $\overline{\text{WDO}}$ to reset the microprocessor. This can be done by connecting $\overline{\text{WDO}}$ to $\overline{\text{RES}}$. If the pins try to drive to different output levels, the low output level dominates. Additional current flows from VDD to GND during these states. If the application cannot support additional current (during fault conditions), $\overline{\text{RES}}$ and $\overline{\text{WDO}}$ can be connected to the inputs of an OR gate whose output is connected to the microprocessor's reset pin.

LAYOUT CONSIDERATIONS

A 0.1-μF capacitor connected from VDD to GND is recommended to decouple the UCCx946 from switching transients on the VDD supply rail.

Since RP and WP are precision current sources, capacitors C_{RP} and C_{WP} should be connected to these pins with minimal trace length to reduce board capacitance. Care should be taken to route any traces with high voltage potential or high speed digital signals away from these capacitors.

Resistors R1 and R2 generally have a high ohmic value, traces associated with these parts should be kept short in order to prevent any transient producing signals from coupling into the high impedance RTH pin.

TYPICAL CHARACTERISTICS

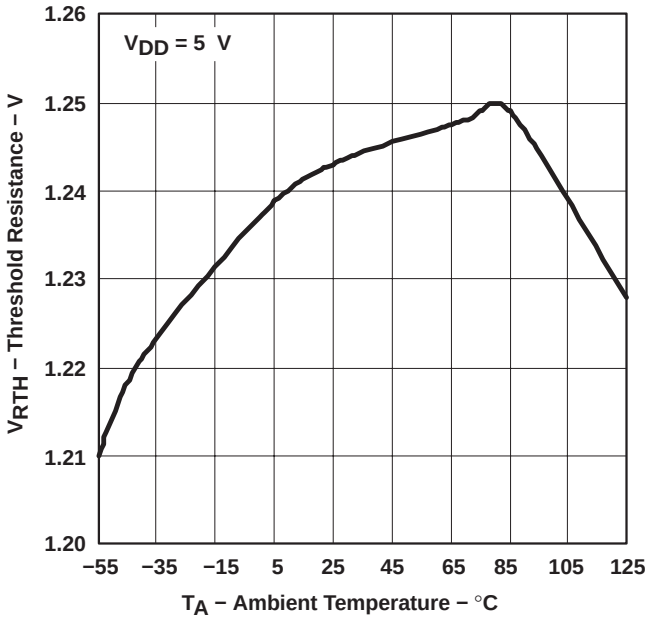


Figure 5.

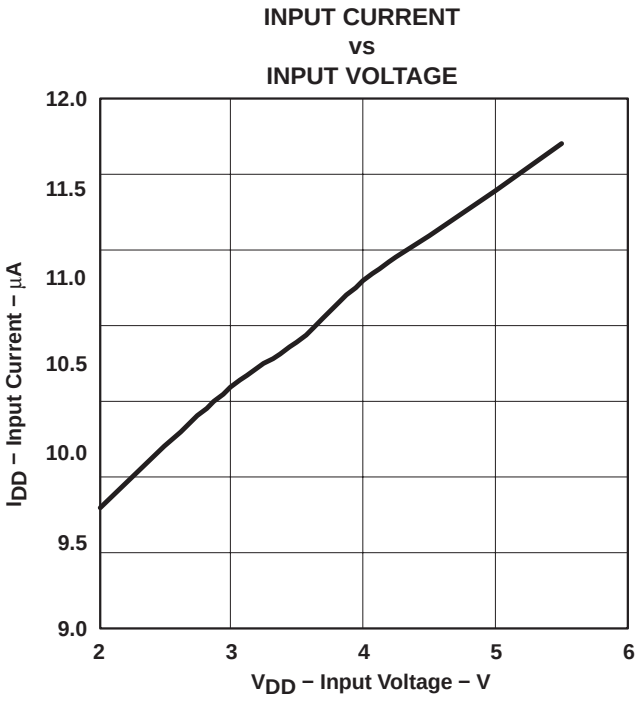


Figure 6.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2946D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2946	Samples
UCC2946DG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2946	Samples
UCC2946DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2946	Samples
UCC2946DTRG4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2946	Samples
UCC2946PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2946	Samples
UCC2946PWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2946	Samples
UCC2946PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2946	Samples
UCC2946PWTRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2946	Samples
UCC3946D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3946	Samples
UCC3946DTR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3946	Samples
UCC3946N	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3946N	
UCC3946NG4	LIFEBUY	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3946N	
UCC3946PW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3946	Samples
UCC3946PWTR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3946	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF UCC2946 :

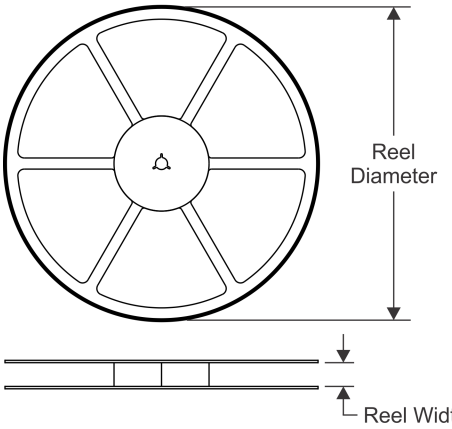
- Automotive: UCC2946-Q1

NOTE: Qualified Version Definitions:

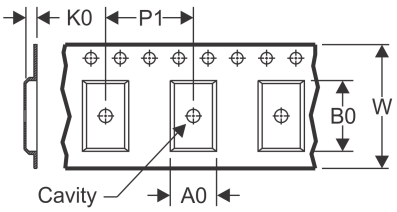
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

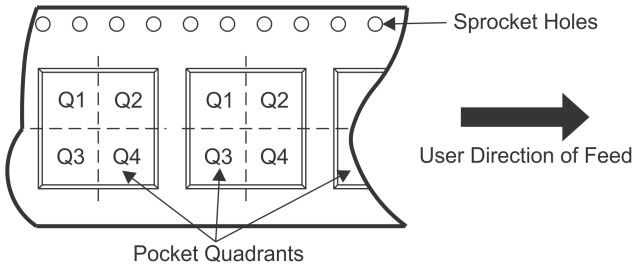


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

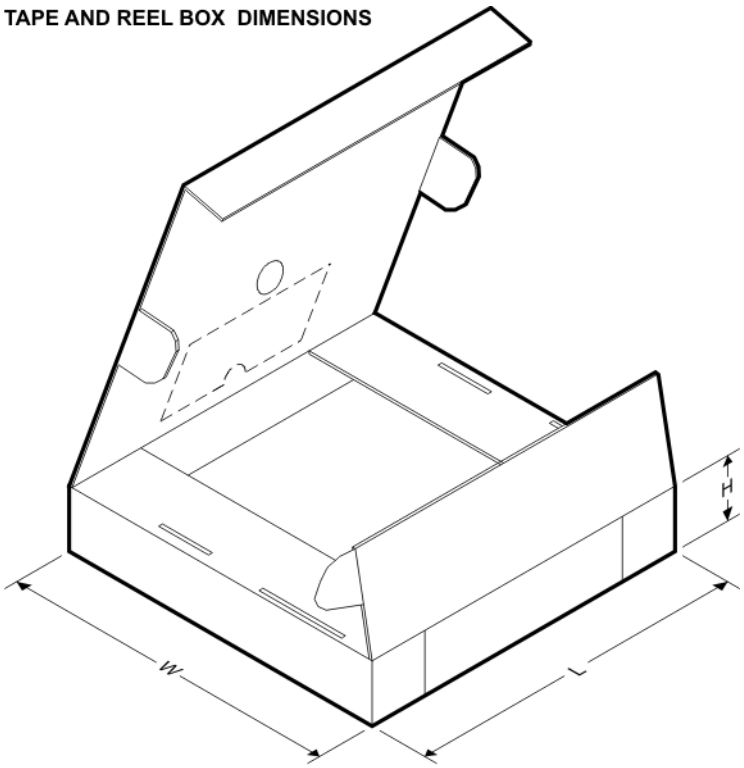
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2946DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2946PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
UCC3946DTR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3946PWTR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

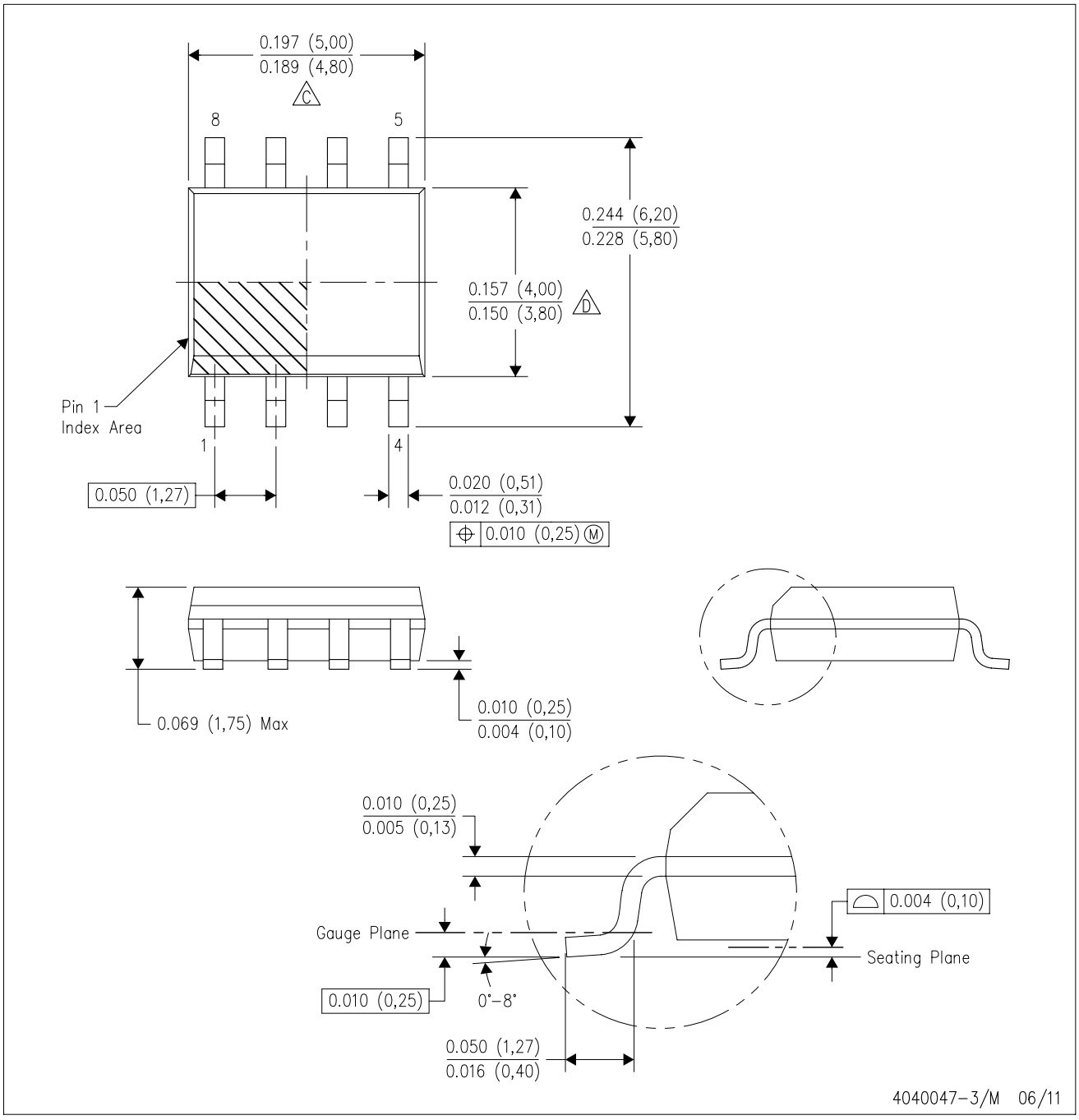
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

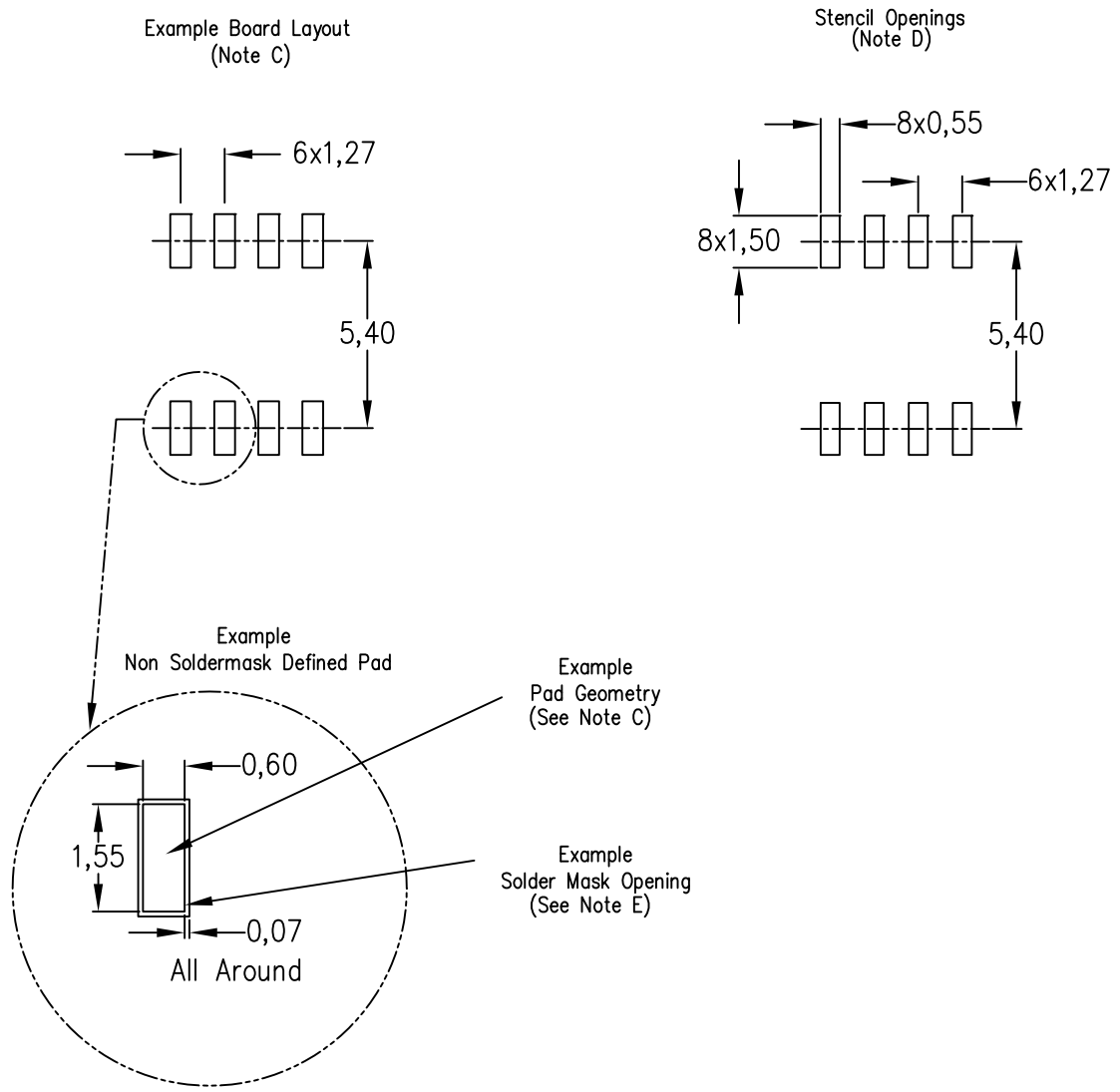
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2946DTR	SOIC	D	8	2500	367.0	367.0	35.0
UCC2946PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0
UCC3946DTR	SOIC	D	8	2500	367.0	367.0	35.0
UCC3946PWTR	TSSOP	PW	8	2000	367.0	367.0	35.0

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



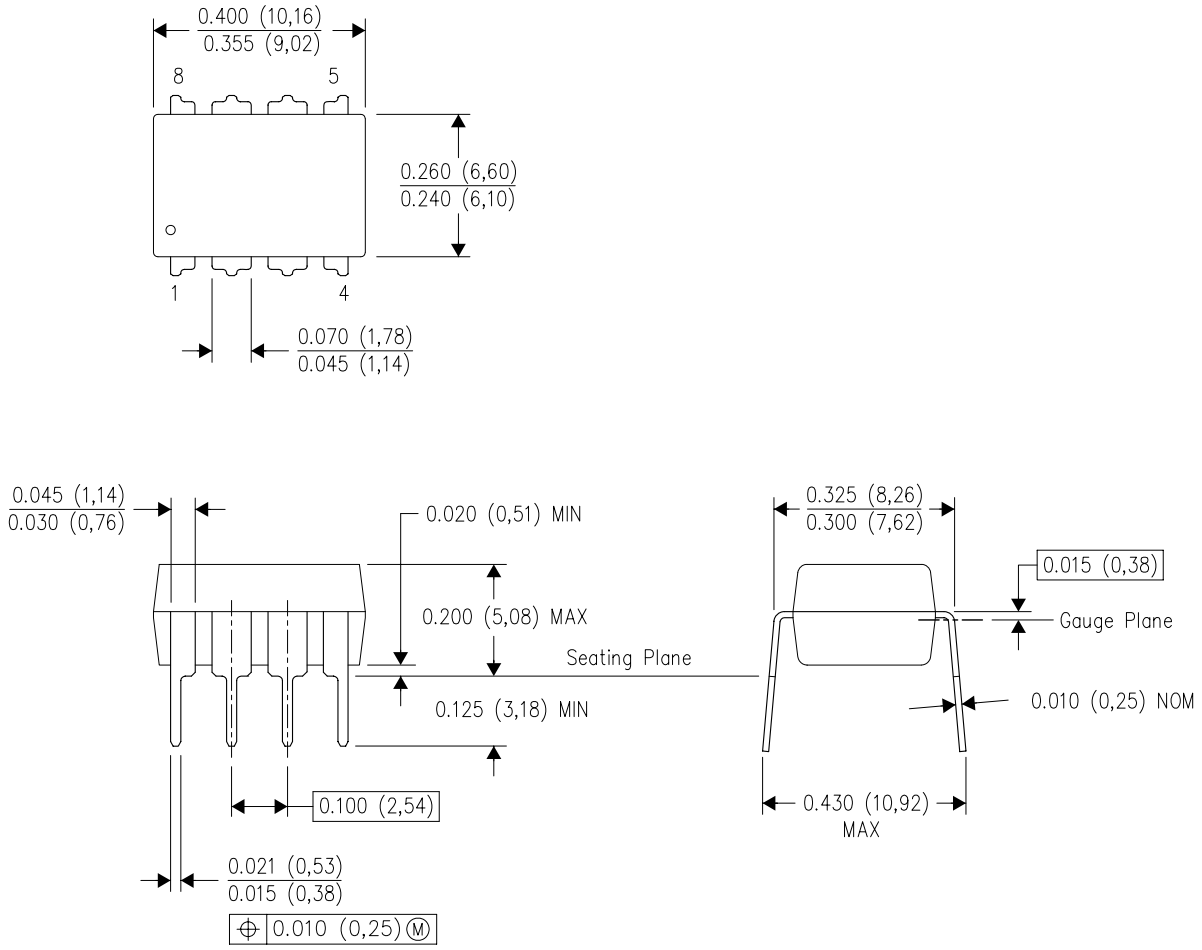
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AA.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



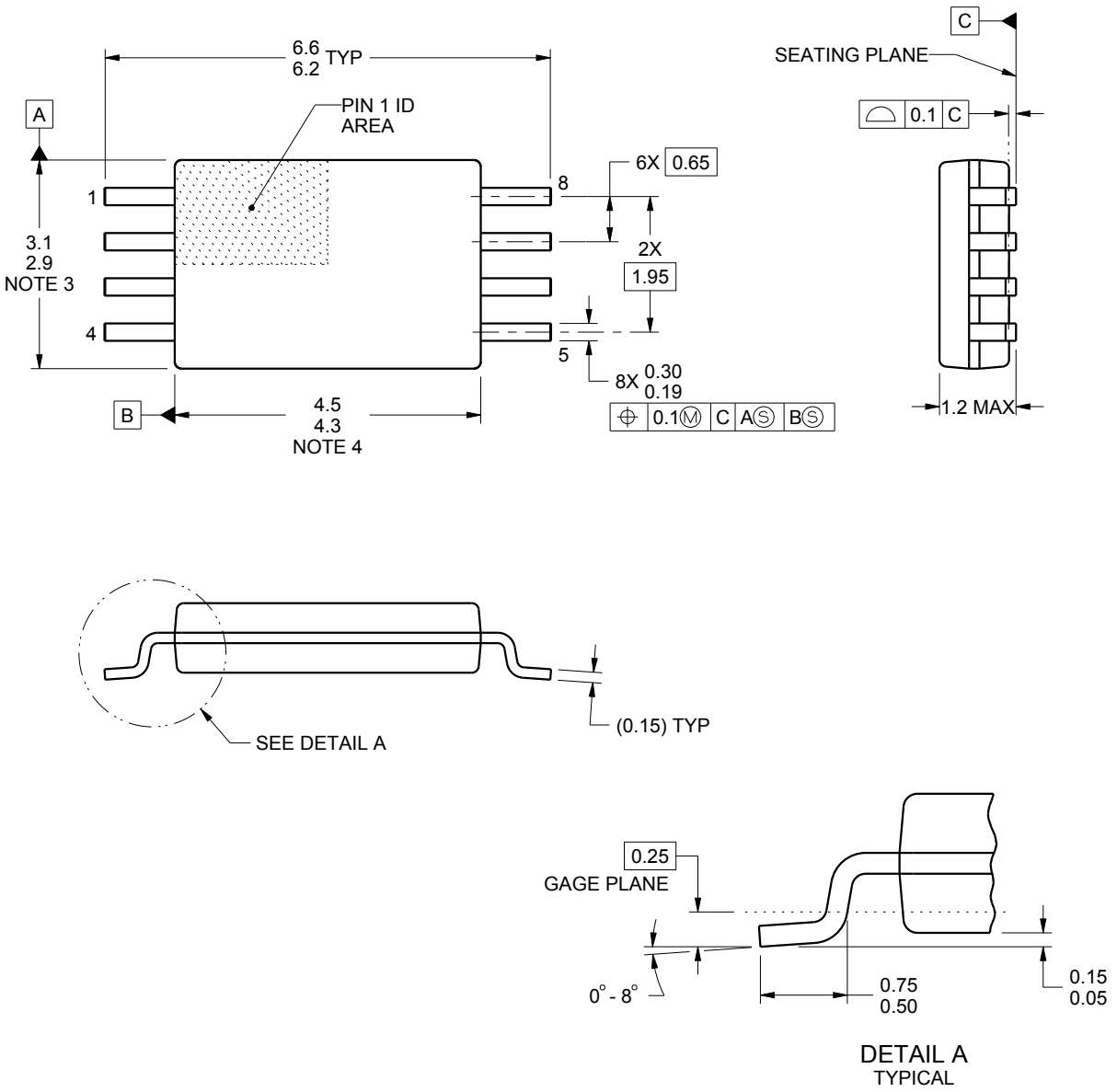
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

PACKAGE OUTLINE

PW0008A

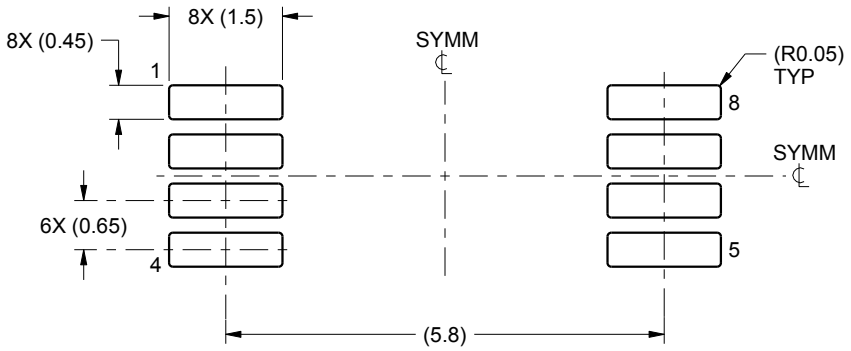
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

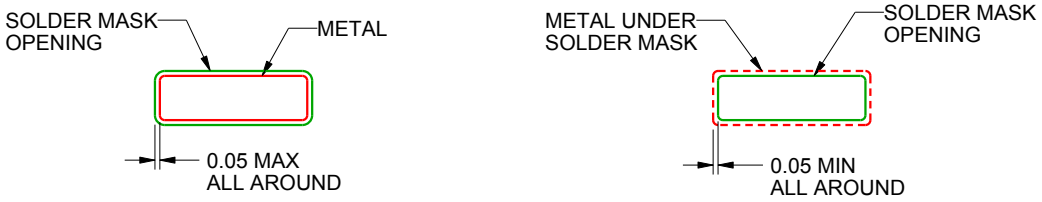


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X



SOLDER MASK DETAILS
NOT TO SCALE

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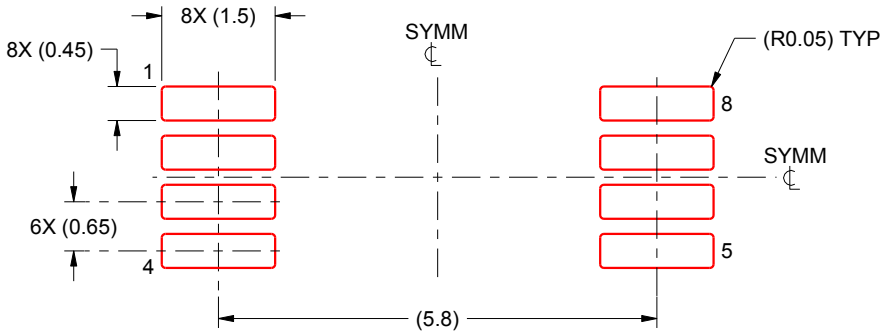
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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